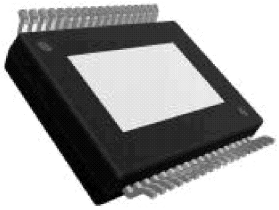
Power management system IC

- Two 5V low-drop voltage regulators (250mA, 100mA continuous mode
- Low stand-by current: V_{BAT} stby, 7µA; V_1 stby, 45µA, (75µA in cycl. sense)
- Window watchdog and fail-safe output
- Interrupt output
- Wake-up logic with cyclic contact monitoring
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- 24 bit SPI interface for mode control and diagnostic
- Output drivers
- 4 High side drivers for e.g. LED or HALL ($R_{DSon,typ}$ = 7 Ω)
- 1 High side driver Out_HS ($R_{DSon,typ}$ = 1 Ω)
- 2 Relay drivers ($R_{DSon,typ}$ = 2 Ω)
- Outputs are short circuit protected
- 2 Op amp's for current sensing in GND return lines
- Temperature warning and thermal shutdown



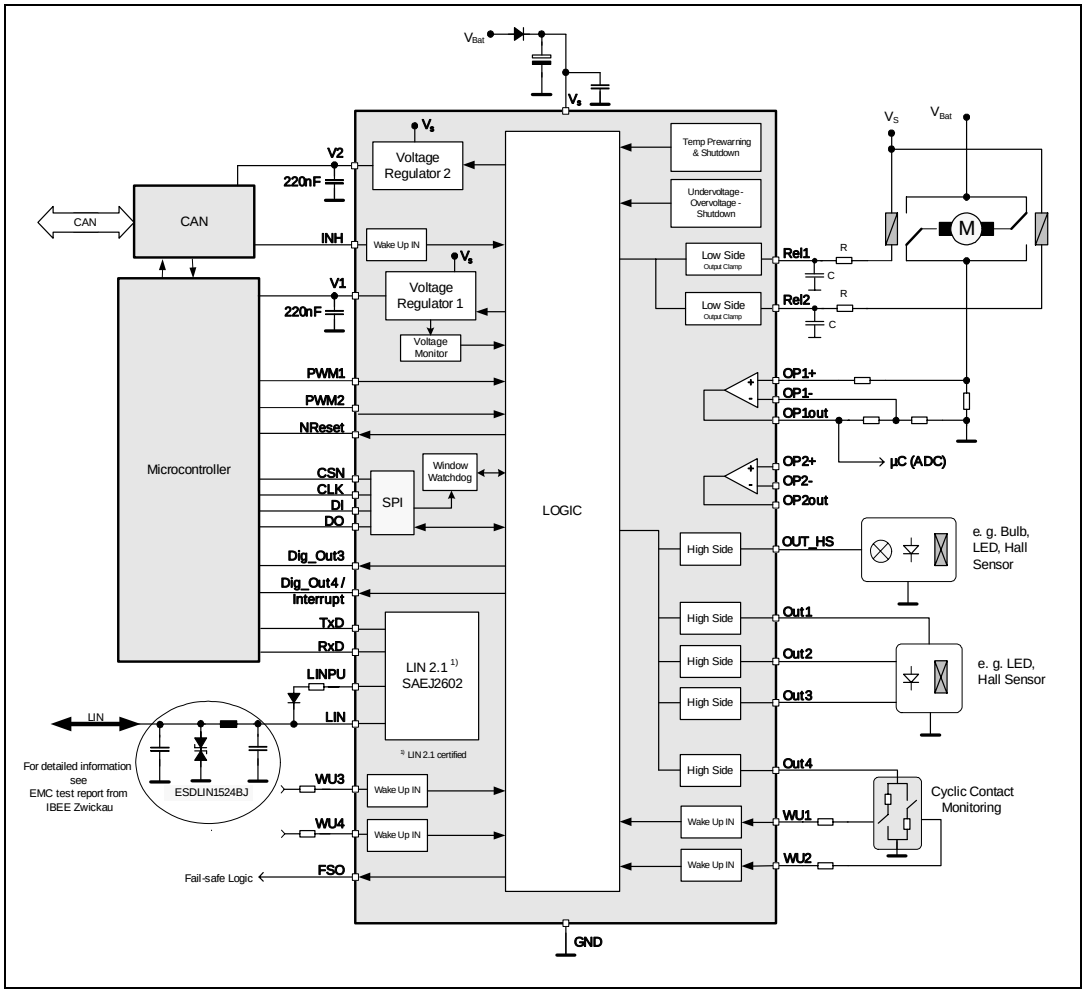
PowerSSO-36

- Automotive ECU' s such as door zone and body control modules.

The L9952GXP is a power management system IC containing two low drop regulators with advanced contact monitoring and additional peripheral functions.

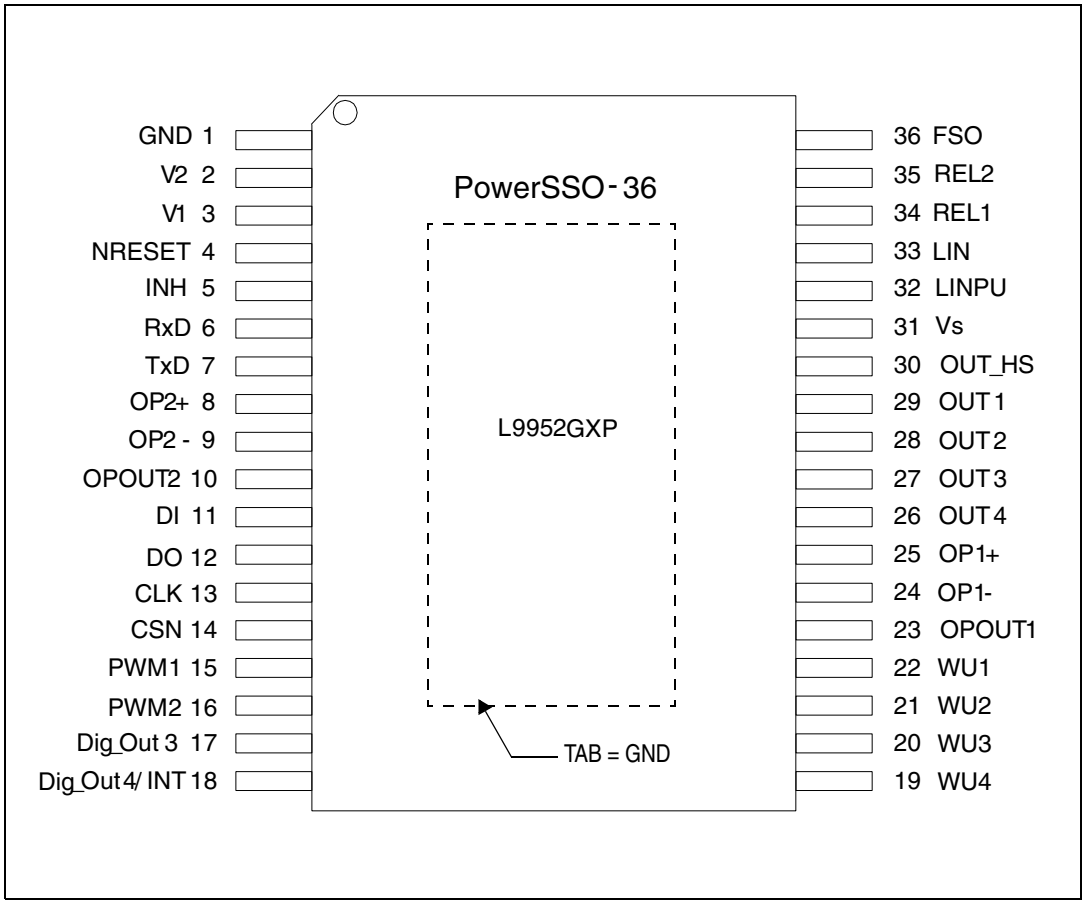
The integrated standard serial peripheral interface (SPI) controls all L9952GXP operation modes and provides driver diagnostic functions.

PowerSSO-36	L9952GXP	L9952GXPTR



GND	1	Ground
V2	2	Voltage regulator 2 output : 5 V supply for external loads e.g. IR receiver, potentiometer
V1	3	Voltage regulator 1 output : 5 V supply e.g. micro controller, Can transceiver
NReset	4	NReset output to micro controller - Internal pull-up of typ. 100KΩ (reset state = low)
INH	5	Wake-up input e.g. from CAN transceiver
RxD	6	Receiver output of the LIN 2.1 transceiver

TxD	7	Transmitter input of the LIN 2.1 transceiver
OP2+	8	Non inverting input of operational sense amplifier
OP2-	9	Inverting input of operational sense amplifier
$OP2_{OUT}$	10	Output of operational sense amplifier
DI	11	SPI : serial data input
DO	12	SPI : serial data output
CLK	13	SPI : serial clock input
CSN	14	SPI : chip select not input
PWM1	15	Pulse width modulation input
PWM2	16	Pulse width modulation input
Dig_Out3	17	Digital output
Dig_Out4/INT	18	Digital output (configurable as Interrupt Output)
$Wu_{4..1}$	19 to 22	Wake-up input: input pins for static or cyclic monitoring of external contacts
$OP1_{OUT}$	23	Output of operational sense amplifier
OP1-	24	Inverting input of operational sense amplifier
OP1+	25	Non inverting input of operational sense amplifier
$Out_{4..1}$	26 to 29	High side driver (7 Ω, typ.) - to supply e.g. LED' s, HALL sensors or external contacts
Out_HS	30	High side drivers (1 Ω, typ.) - to supply e.g. LED' s, Bulbs, HALL sensors or external contacts
Vs	31	Power supply voltage
LINPU	32	LIN master pull up
LIN	33	LIN bus line
Rel1	34	Low side driver (2 Ω, typ.) - e.g. relay
Rel2	35	Low side driver (2 Ω, typ.) - e.g. relay
FSO	36	Fail safe output - used to supervise or control applications in case of watchdog and/or V1 under-voltage failure (e.g. to activate emergency lights)


PowerSSO-36
L9952GXP
TAB = GND
GND 1
V2 2
V1 3
NRESET 4
INH 5
RxD 6
TxD 7
OP2+ 8
OP2 - 9
OPOUT2 10
DI 11
DO 12
CLK 13
CSN 14
PWM1 15
PWM2 16
Dig_Out 3 17
Dig_Out 4/ INT 18
36 FSO
35 REL2
34 REL1
33 LIN
32 LINPU
31 Vs
30 OUT_HS
29 OUT 1
28 OUT 2
27 OUT 3
26 OUT 4
25 OP1+
24 OP1-
23 OPOUT1
22 WU1
21 WU2
20 WU3
19 WU4

The L9952GXP contains 2 independent and fully protected low drop voltage regulators, which are designed for very fast transient response.

The output voltage is stable with loads capacitors $\geq$ 220nF.

The voltage regulator V1 provides 5V supply voltage and up to 250mA continuous load current for the external digital logic (micro controller, CAN transceiver ...). In addition the regulator V1 drives the L9952GXP internal 5V loads. The voltage regulator is protected against overload and over-temperature. An external reverse current protection has to be provided by the application circuitry to prevent the output capacitor from being discharged by negative transients or low input voltage. The output voltage precision is better than +/-2% (incl. temperature drift and line-/load regulation) for operating mode; respectively +/-3% during low current mode. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors $\geq$ 220nF.

If device Temperature exceeds TSD1 threshold, all outputs (Hsx, Lsx, V2, LIN) will be deactivated except V1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2>TSD1), also V1 will be deactivated (see state chart Fig. 3.1: “Protection and diagnosis”). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1sec. During this time, all other wakeup sources (CAN, LIN, and WU1...4) are disabled. After 1 sec, the voltage regulator will try to restart automatically. If TSD2 occurs within one minute and for 8 consecutive times, the L9952GXP enters the V_{BAT} - standby mode.

In case of short to GND at “V1” after initial turn on (V1 < 2V for at least 4ms) the L9952GXP enters the V_{BAT} - standby mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..4, SPI.

The voltage regulator V2 supplies additional 5V loads (e.g. Logic components, external sensors, external potentiometers). The continuous load current is 50mA. The regulator provides accuracy better than $\pm$ 3% @ 50mA (4% @ 100mA) load current.

In case of short to GND at “V2” after initial turn on (V2 < 2V for at least 4ms) the V2 regulator is switched off. Micro processor has to send a clear command to reactivate the V2 regulator.

V2 is protected against:

- Overload
- Over temperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

The L9952GXP can be operated in 4 different operating modes:

- Active
- Flash
- V_1- standby
- V_{BAT} - standby

A cyclic monitoring of wake-up inputs is available in stand-by modes.

All functions are available.

To disable the watchdog feature a FLASH program mode is available.

The mode can be entered by $V_{PWM2} \geq 9V$

In this case all other functions are the same as in active mode

Watchdog can be disabled as well as soon as L9952GXP enters the V1 standby mode (see section 2.9 for details)

Note: *"High" level for flash mode selection is $V_{PWM2} \geq 9V$. For all other operation modes, standard 5V logic signals are required. For proper operation PWM1 must not be set to a voltage level above standard 5V logic.*

Outputs and internal loads are switched off. To supply the micro controller in a low power mode, the voltage regulator1 (V1) remains active. The intention of the V1 standby mode is to preserve the RAM contents. A cyclic contact supply and wake-up input sense feature (for cyclic monitoring of external contacts) can be activated by SPI.

To achieve minimum current consumption during V_{BAT} standby mode, all L9952GXP functions (except the ones for wake up functionality) are switched off.

In V_{BAT} - standby mode the current consumption of the L9952GXP is reduced to 7µA, typical (without cyclic sense feature selected).

The transitions from active mode to either V_1-standby or V_{BAT} - standby are controlled by SPI.

V_{BAT} - standby mode is dominant; i.e. if both bits, V_1 - standby and V_{BAT} - standby are set to "1", the L9952GXP will enter V_{BAT} - standby mode.

A wake-up from standby mode will switch the device to active mode. This can be initiated by one or more of the following sources:

- Change of the LIN state at LIN bus interfaces
- A current at the INH pin (I ≥200uA) controlled by the CAN-transceiver (the CAN transceiver is not a part of the IC).
- Positive/negative edge at wake up pins WU1...WU4 -> change of level after going into stand-by
- Change of open-load state at OUT1 to 4
- SPI access in V1-standby mode (CSN is low and first rising edge on CLK)

LIN	Always active
INH	Always active
WU1...4	Can be individually disabled via SPI
Open Load at HS outputs	Can be individually disabled via SPI
SPI Access	Always active (except in V_{BAT} - standby mode)
High level at PWM2 input	VPWM2 > 9V (1)

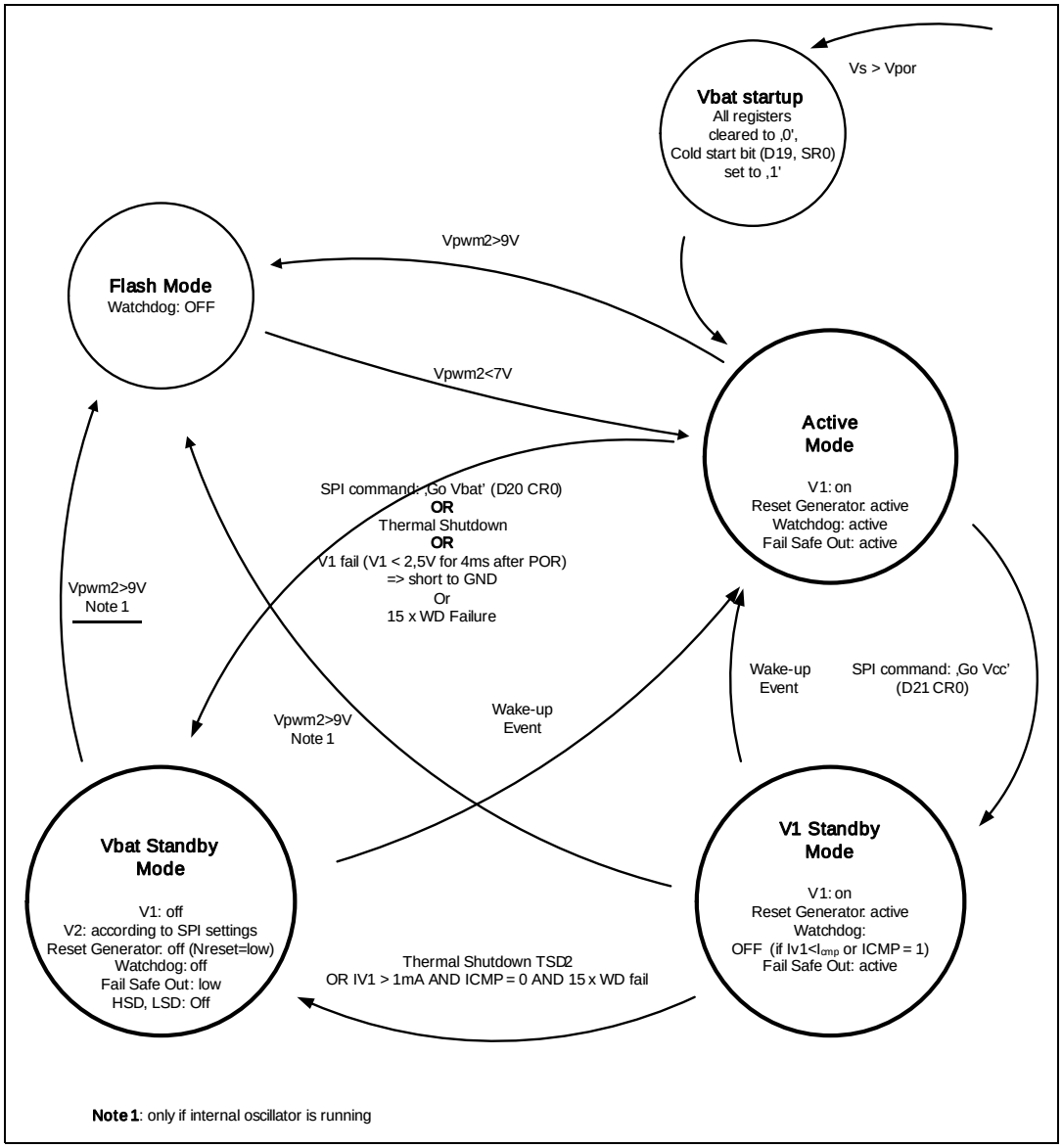
1. Only if internal oscillator is running (e. g. in cyclic sense configuration or after wake-up request).

All wake-up events (except wake-up by LIN, INH or SPI from V1standby mode) generate a Reset pulse (NReset low for 2ms).

Wake-up events from V1standby by LIN, INH or SPI do not cause a Reset and the Reset generation is blocked for 2ms, i. e. a watchdog failure during this timeframe will not cause a reset.

2.3.1	Voltage-regulator, V1	VOUT= 5V	On	On (1)	Off
2.3.2	Voltage-regulator, V2	VOUT= 5V	On / Off (2)	On (2) / Off	On (2) / Off
2.3.3	Reset-generator		On	On	Off
2.3.4	Window watchdog	V_1 monitor	On	Off if (I_V1 < I_{CMP} and I_{CMP}=0) or I_{CMP} = 1	Off
2.3.5	Wake up		Off (3)	Active (4)	Active (4)
2.3.6	HS-cyclic supply	Oscillator timebase	On / Off	On (2) / Off	On (2) / Off
2.3.7	Relay driver		On	Off	Off
2.3.8	Operational amplifiers		On	Off	Off
2.3.9	LIN line driver	LIN 2.1	On	Off	Off
2.3.10	LIN line receiver		On	On	On
2.3.11	FSO	Fail-safe output	Hi – no error Lo – WD or V1 fail	Hi – no error Lo – WD or V1 fail (5)	Lo -> because V1= off
2.3.12	Oscillator		On	(6)	(6)
2.3.13	Vs-Monitor		On	(7)	(7)

1. Supply the processor in low current mode
2. Only active when selected via SPI
3. Input Status can be read by SPI (Status Register 0); Inputs should be configured for static sense (Control Register 2)
4. Unless disabled by SPI
5. Watchdog is active in V1 standby mode, until I(V1) is below I_{CMP} current threshold
6. Activation = ON if cyclic sense is selected
7. Cyclic activation = pulsed ON during cyclic sense


Vbat startup
All registers
cleared to ‚0',
Cold start bit (D19, SR0)
set to ‚1'
Vs > Vpor
Flash Mode
Watchdog: OFF
Vpwm2>9V
Vpwm2<7V
Active
Mode
V1: on
Reset Generator: active
Watchdog: active
Fail Safe Out: active
SPI command: ‚Go Vbat' (D20 CR0)
OR
Thermal Shutdown
OR
V1 fail (V1 < 2,5V for 4ms after POR)
=> short to GND
Or
15 x WD Failure
Vpwm2>9V
Note 1
Wake-up
Event
SPI command: ‚Go Vcc'
(D21 CR0)
Vpwm2>9V
Note 1
Wake-up
Event
Vbat Standby
Mode
V1: off
V2: according to SPI settings
Reset Generator: off (Nreset=low)
Watchdog: off
Fail Safe Out: low
HSD, LSD: Off
V1 Standby
Mode
V1: on
Reset Generator: active
Watchdog:
OFF (if Iv1<Iomp or ICMP = 1)
Fail Safe Out: active
Thermal Shutdown TSD2
OR IV1 > 1mA AND ICMP = 0 AND 15 x WD fail
Note 1: only if internal oscillator is running

The de-bounced digital inputs WU1...WU4 can be used to wake up the L9952GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 µs is implemented at WU1-4. The filter is started when the input voltage passes the specified threshold. At Vin > 1V and Vin < (Vs – 2V), a Wake-up request is processed. During Wake-up request, the internal oscillator and other circuit blocks are activated in order to allow more accurate monitoring of the inputs.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic wake up feature is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer 1 (0.5sec to 4.0sec in 0.5sec steps) or Timer 2 (50ms). The input signal is filtered with a filter time of 16us after a programmable delay (80us or 800us). A Wake-up will be processed if the status has changed versus the previous cycle.

The Outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timing according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode (Icxx in control register 2), the same input filter timing (Timer1 or Timer2) and the corresponding input filter delay (control register 2) must be used for the HS Outputs (Hsxx in control register 0) which supply the external contact switches.

In Standby mode, the inputs WU1-4 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external contacts (pull-up for active low contacts, pull-down for active high contacts). In active mode the inputs have a pull down resistor of 100 kOhm (typ).

In Active mode, the input status can be read by SPI (Status Register 0). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

Applications like Hall sensor outputs need high processing speed. The 12V signals connected to the wakeup inputs WU3 and WU4 can be looped through to the digital outputs Dig_Out 3 and Dig_Out 4 (5V) in order to avoid read out of the input state by SPI.

The setup is programmable by SPI.

The open load states of the High Side Drivers OUT1 and OUT2 can be looped through the digital outputs Dig_Out3 and Dig_Out4 without delay. In addition, the status of OUT1 and OUT2 can be accessed through the SPI interface. This feature is intended for 2-pin HALL sensors. Open Load information is only valid during ON state.

The Open Load threshold at pins OUT1...4 can be switched from I_{OLD1} = 2mA to

I_{OLD2} = 8 mA via SPI .

Dig_Out4 can be configured via SPI as Interrupt output (INT) by setting Bit 20 / CR1:INT_enable='1'.

This configuration will enable the following behaviour:

- INT pin is pulled high for 2ms in case of any wake-up from V1 standby mode (WU inputs, LIN, INH, SPI, open load HS, Iv1 > I_{CMP}_ris)
- Wake-up events from V1 standby do not generate a reset (i.e. NRESET is not pulled low)
- The Dig_Out4 settings in CR1 (Bits 12..14) will be ignored

In V1 and V_{BAT} standby mode, any high side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X sec, the on-time is 10ms resp. 20ms

With X ∈ {0.5, 1.0, 1.5, ... 4 }

Timer 2: period is 50ms, the on- time is 100us resp. 1ms:

Note: Cyclic sense setup: if cyclic sense feature is used for wake-up inputs (Icxx in control register 2), same input filter timing (Timer1 or Timer2) must be used for HS Outputs (Hsxx in control register 0).

During normal operation the watchdog monitors the micro controller within a nominal trigger cycle of 10ms.

In V_{BAT} -standby , V1-standby and Flash program modes, the watchdog circuit is automatically disabled. However, the watchdog will remain enabled in V1-standby mode until the current at V1 decreases below I_{CMP}_fall. The V1 current monitoring can be disabled, if the I_{CMP} bit (CR2, D20) is set to '1'.

After 'power-on', 'standby mode' or reset, the window watchdog starts with a long open window (65ms). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is finally accepted when the CSN input becomes HIGH after the transmission of the SPI word.

A correct watchdog trigger will start the window watchdog with a closed window (< 6ms) followed by an open window (< 10ms), see timing diagrams. Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit (CR0, D19). The "negative" or "positive" edge has to meet the open window time. A correct watchdog trigger signal will immediately start the next closed window.

After 8 watchdog failures in sequence, the V1 regulator is switched off for 200ms. In case of 7 further watchdog failures, the V1 regulator is completely turned off and the device goes into V_{BAT} standby mode until a wakeup occurs. (e.g. via LIN, CAN/INH).

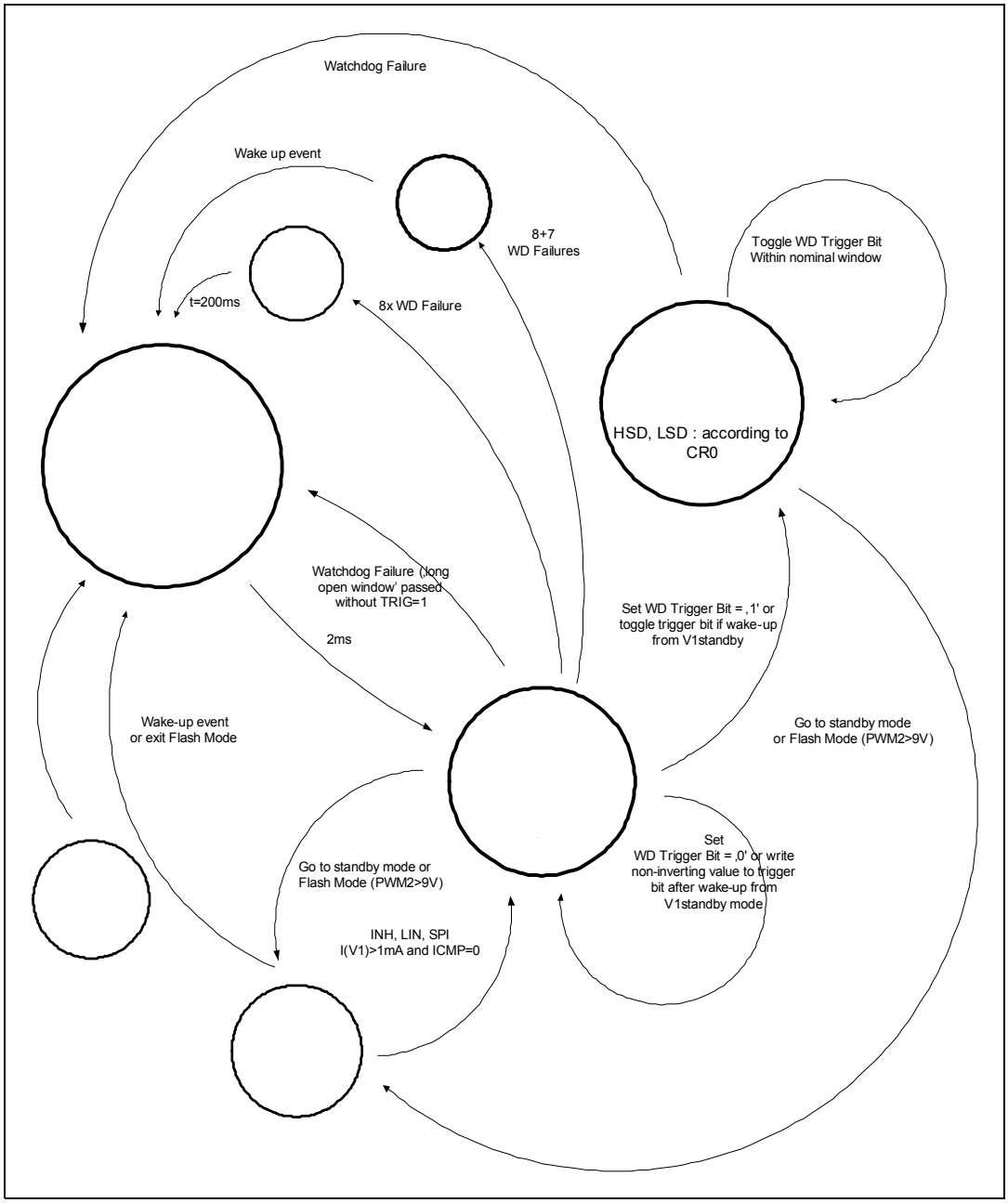
The watchdog is triggered by toggling the trigger bit (CR0, D19).

Note: The active trigger window will be reset after each correct trigger write operation.

In case of reset (NReset low for 2ms) the trigger bit is set to "0".

In case of a WD failure, the outputs (Lsx, Hsx, V2) are switched off and NReset is pulled low for 2ms.

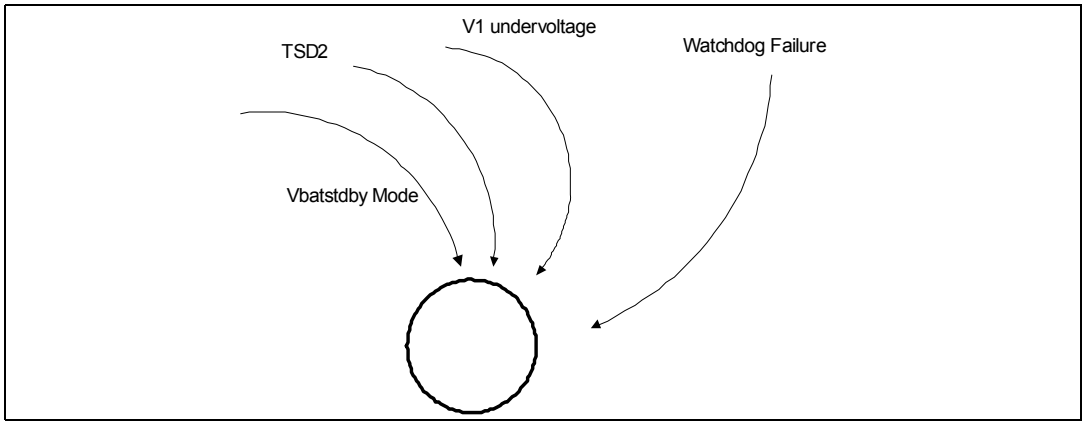
Writing to control register 0 without inverting the WD trigger bit is possible at any time.



After power-on (Vs > V_{POR}) or wakeup from V_{BAT} -standby mode, the output FSO is set to “HIGH”, if V1 is above the V1 threshold. FSO is set to “LOW” in case of V1 under voltage or watchdog failure.

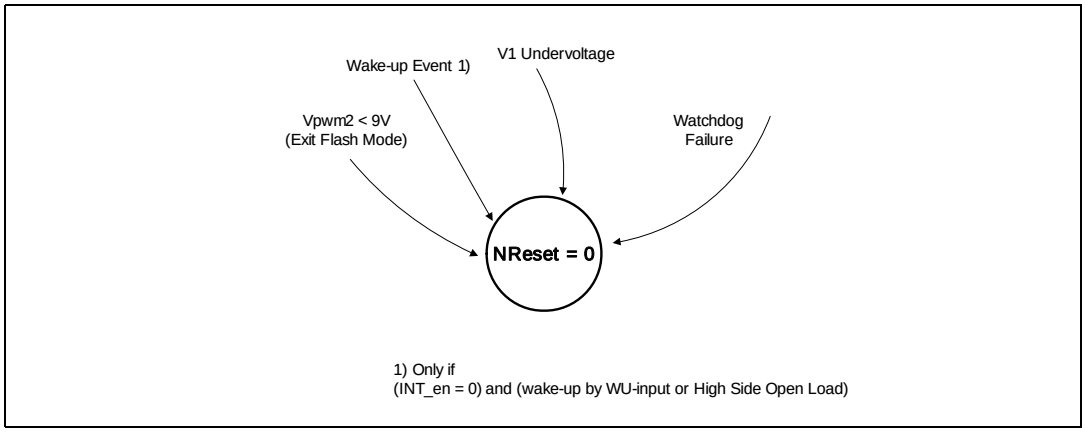
During V1-standby mode, FSO is HIGH unless a V1 under-voltage or watchdog reset occurs. WD remains enabled in V1 standby mode until I_{V1} drops below 150uA. In V_{BAT} - standby mode, FSO is low. At exit from V_{BAT} - standby mode, it goes to high as soon as V1 is stable.

At wakeup FSO remains high, provided that the watchdog is triggered successfully. It is set low if the watchdog is not served during the long open window of if a V1 under-voltage occurs.



IF V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output “NRESET” is switched to “HIGH” after a 2ms reset delay time. This is necessary for a defined start of the micro controller when the application is switched on.

As soon as an under voltage condition of the output voltage (V1 < VRT) for more than 8us appears, the reset output is switched low again.



The $V_{1,}$ and V_2 regulator output voltages are monitored.

In case of a drop below the $V_{1,}$ V_2 – fail thresholds ($V_{1,2}$ < 2V,typ for t > 2us), the $V_{1,2}$ - fail bits are latched. The fail bits are cleared by a dedicated SPI command.

If 4ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for V1,2), the L9952GXP will identify a short circuit condition at the related regulator output and the regulator will be switched off.

In case of a V1 failure the device enters V_{BAT} - standby mode automatically.

In case of a V2 failure the SHT5V2 bit (SR0 Bit12) is set.

The outputs Rel1, Rel2 (R_{DSon} = 2 Ω typ. @25 °C) are specially designed to drive relay loads.

Typical relays used have the following characteristics:

Relay type 1:

- closed armature: R = 160 Ω ±10%, L= 300mH
- open armature: R = 160 Ω ±10%, L= 240mH

Relay type 2:

- closed armature: R= 220 Ω ±10%, L= 420mH
- open armature: R= 220 Ω ±10%, L= 330mH

The outputs provide an active output zener clamping (40V) feature for the demagnetisation of the relay coil, even though a load dump condition exists. In case of watchdog failure the relay drivers will be switched off and the low side driver control bits are cleared.

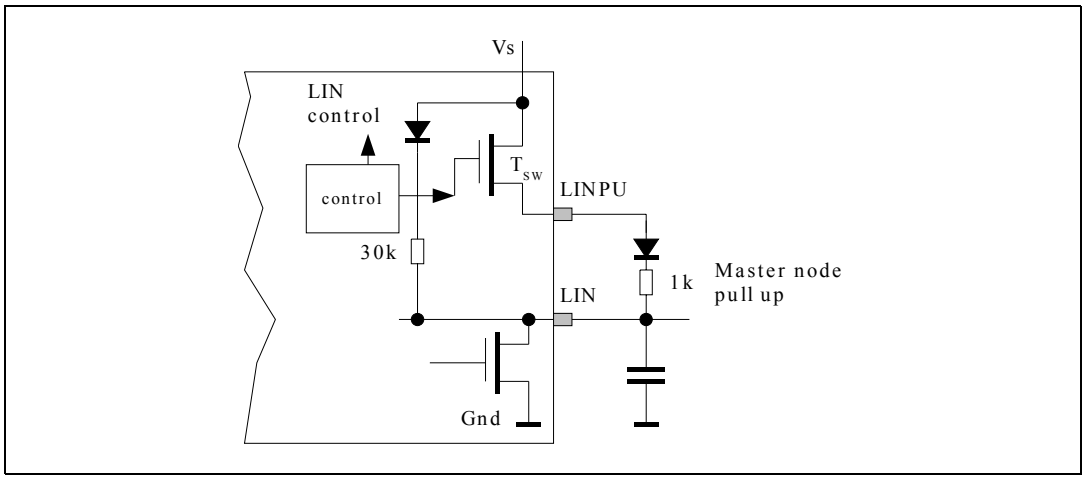
Note: 1 Due to relays bouncing, high dV/dt and/or dI/dt transients may occur on the low side driver outputs. In case high currents are switched (for example window lift motor), due to parasitic capacitive inductive coupling from load side of relays to the relays coils, the Absolute Maximum Ratings of the Low Side driver outputs may be exceeded. In order to avoid this, it is recommended to place a 10nF capacitor at the Rel1, Rel2 outputs to GND.

2 If a hard short circuit to V_{BAT} is possible at the "Low Side Driver" outputs, an RC network is required with T_{RC} > 1µs, R ≥ 1 Ω (see block diagram, the value is given for an output short circuit of given di/dt = 5A/µs).

The inputs PWM 1,2 can be used to control the output drivers Out1..4 and OUT_HS with a PWM signal. Each PWM input can be mapped individually to each of the above listed outputs according to the SPI settings.

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes - 0.2 ... 3V.

The operational amplifiers are designed for GND + 3V... GND – 0.2V input voltage swing and rail-to-rail output voltage range. All Pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.



A dedicated built-in switch “Tsw” enables the LIN to act as a master. (see chapter 2.18)

General requirements:

- Speed communication up to 20kbit/s
- LIN 2.0 compliant (SAEJ2602 compatible) transceiver
- Function range from +40V to -18V DC at LIN Pin
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller Interface with CMOS compatible I/O pins.
- Pull up resistor internal.
- ESD: immunity against automotive transients per ISO7637 specification (see application note)
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

The L9952GXP provides the following 3 error handling features which are not described in the LIN Spec. V2.1, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

If TXI is in dominant state (low) for more than 12ms (typ) the transmitter will be disabled until TXI becomes recessive (high). This feature can be disabled via SPI.

If TXI changes to dominant (low) state but RXI signal does not follow within 40µs, the transmitter will be disabled until TXI becomes recessive (high).

A wake up caused by a message on the bus will start the voltage regulator and the micro controller to switch the application back to normal operation mode.

In standby mode the L9952GXP can receive a wake up from LIN bus. For the wake up feature the L9952GXP logic differentiates two different conditions.

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for at least 40µs, will switch the L9952GXP to active mode.

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for at least 40us, will switch the L9952GXP to active mode.

In V1 standby condition the RxD is a tristate pin.

The LINPU (LIN pull up) signal is set by L9952GXP logic in order to drive the LIN transceiver in master mode. The master mode is realized by an internal high side switch and an external diode in series with an external 1k resistor. In master mode the high side switch is closed causing an external pull up path in parallel to the internal one (diode & 30k resistor).

HS (high side) characteristics:

- HS does not have an over current protection.
- The HS remains active in standby mode.
- Switch off only in case of over temperature (TSD2 = thermal shutdown #2).
- Typical R_{DSon}, 10 Ω.

The Linpu is activated by default (LIN master mode) and can be switched off with a SPI command (see register 2) to reduce current in case of LIN shorted to ground.

A 24 bit SPI command (2 adresses + 22 data bits) is used for bi-directional communication with the micro controller.

During active mode, the SPI:

1) triggers the watchdog

2) controls the modes and status of all L9952GXP modules (incl. input and output drivers)

3) provides driver output diagnostic

4) provide L9952 diagnostic (incl. over temperature warning, L9952GXP operation status)

Note: During stand-by modes, the SPI is generally deactivated.

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL=0 and CPHA=0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the global error flag (fault condition) of the device which is a logical -"OR" of all over current, Vs-over / under voltage, temperature warning/shutdown and V1 Fail bits. The micro controller can poll the status of the device without the need of a full SPI-communication cycle.

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 1MHz.

The device has 3 Control registers and 2 Status registers. The first two bits (D22+D23) at the DI-Input are used to select one of the Control registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Control register only if a frame of exact 24 bits is detected. If the Control register 1 is selected for data transfer, the Status register 1 will be transferred to the DO during the current communication frame. For the selection of Control register 0 or Control register 2, the Status register 0 is transferred to DO.

Over and under-voltage detection on Vs.

If the supply voltage Vs reaches the over voltage threshold (V_{SOV})

- The outputs HS1..4, OUT_HS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The over voltage bit is set and can be cleared with the clear bit (CR1,CLR)
- Automatic recovery after Vs over-voltage; selectable via SPI (CR2, bit4)

If the supply voltage Vs drops below the under voltage threshold voltage(V_{SUV})

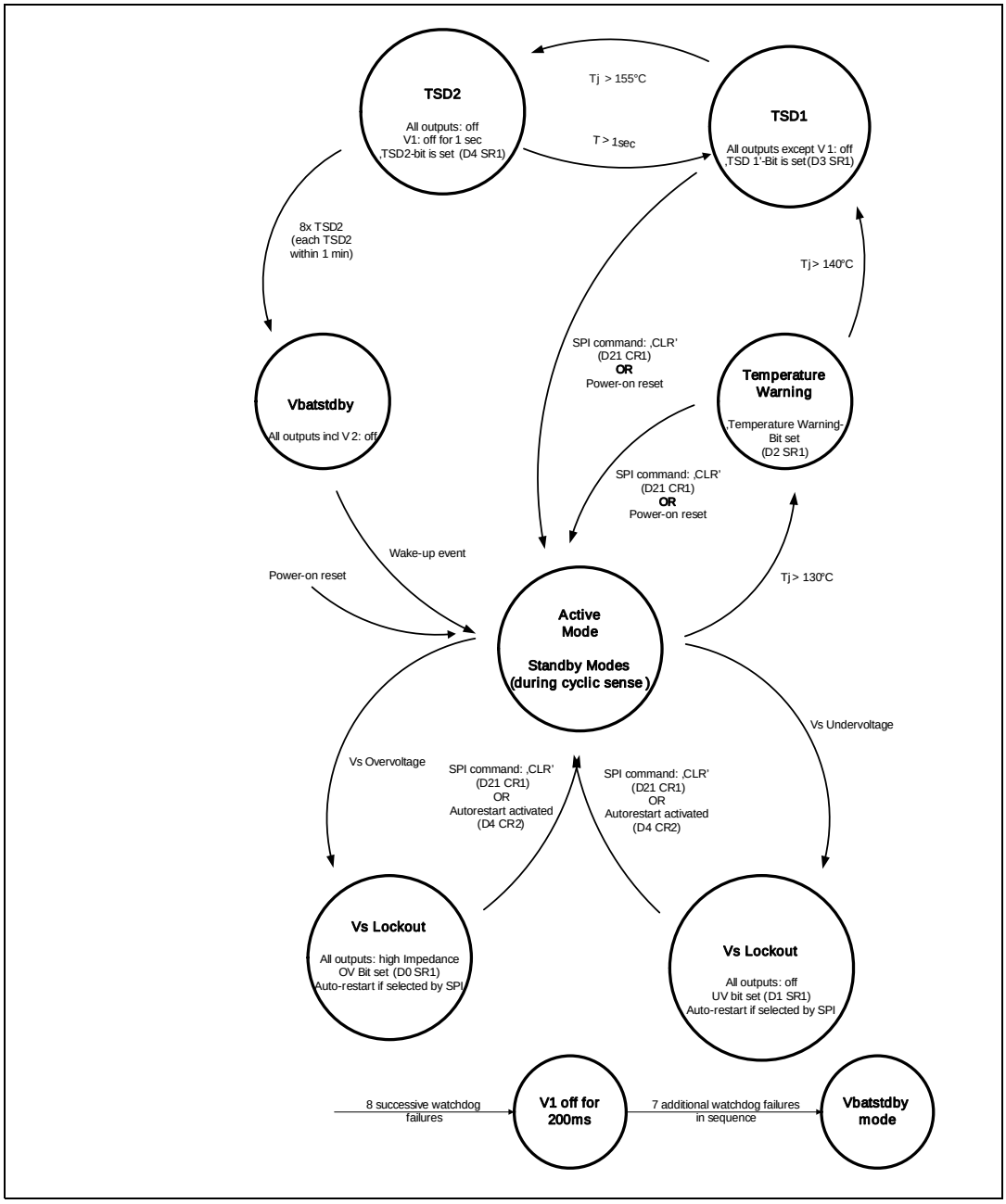
- The outputs HS1..4, OUTHS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The under voltage bit is set
- Automatic recovery after Vs under-voltage; selectable via SPI (CR2, bit4)

See state chart: " Protection and diagnosis".

Digital diagnosis features are provided by SPI:

- V1 reset threshold programmable
- Over temperature including pre warning
- Open load separately for each output stage
- Overload status
- Vs-supply over/under voltage
- V1 and V2 fail bit
- Status of the WU1...4, LIN and INH pin
- Cold start bit
- Number of unsuccessful V1 restarts after thermal shutdown
- Number of sequential watchdog failures
- Status of watchdog trigger bit TRIG: (SR1, Bit 16)
- LIN status (short to ground, short to V_{BAT}, dominant TxD)

See the following state chart: "Protection and diagnosis".


TSD2
All outputs: off
V1: off for 1 sec
,TSD2-bit is set (D4 SR1)
Tj > 155°C
T > 1sec
TSD1
All outputs except V 1: off
,TSD 1'-Bit is set(D3 SR1)
8x TSD2
(each TSD2
within 1 min)
Tj> 140°C
Vbatstdby
All outputs incl V 2: off
SPI command: ‚CLR'
(D21 CR1)
OR
Power-on reset
Temperature
Warning
‚Temperature Warning'-
Bit set
(D2 SR1)
SPI command: ‚CLR'
(D21 CR1)
OR
Power-on reset
Wake-up event
Power-on reset
Tj> 130°C
Active
Mode
Standby Modes
(during cyclic sense)
Vs Undervoltage
Vs Overvoltage
SPI command: ‚CLR'
(D21 CR1)
OR
Autorestart activated
(D4 CR2)
SPI command: ‚CLR'
(D21 CR1)
OR
Autorestart activated
(D4 CR2)
Vs Lockout
All outputs: high Impedance
OV Bit set (D0 SR1)
Auto-restart if selected by SPI
Vs Lockout
All outputs: off
UV bit set (D1 SR1)
Auto-restart if selected by SPI
8 successive watchdog
failures
V1 off for
200ms
7 additional watchdog failures
in sequence
Vbatstdby
mode

The component provides a total of 4 high side outputs Out1...4, (7 Ω typ. @ 25C) to drive e.g. LED' s or hall sensors and 1 high side output OUT_HS with 1 Ω typ. @ 25 C).

The high side outputs are protected against

- Over- and under voltage
- Overload (short circuit)
- Over temperature with pre warning

If the output current exceeds the current shutdown threshold the output transistor is turned off and the corresponding diagnosis bit of the output is set.

The switches are automatically disabled in case of reset condition, Vs-under, Vs-over voltage or thermal shutdown (TSD1&2).

For OUT_HS an auto recovery feature is available in active mode.

If the OUT_HS output current exceeds the current shutdown threshold, the output transistor is turned off and the corresponding diagnosis bit of the output is set.

Via SPI command the auto recovery feature can be enabled in order to restart the driver in case of over current shutdown. This over current recovery feature is intended for loads which have an initial current higher than the over current limit of the output (e.g. Inrush current of cold light bulbs).

The device itself can not distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the micro controller can switch on light bulbs by setting the over current recovery bit for the first 50ms. After clearing the recovery bit, the output will be automatically disabled if the overload condition still exists.

The status of all high side outputs (over-current, open load) can be monitored by SPI interface.

In case of a watchdog failure, the high side drivers are switched off. The control bits are not cleared, i.e. the drivers will go to the previous state once the watchdog failure condition disappears.

ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

Note: Loss of ground or ground shift with externally grounded loads.

The outputs provide an active output zener clamping feature for the demagnetisation of the relay coil, even though a load dump condition exists. For safety reasons the relay drivers are linked with the Watchdog: in case of failure, or missing trigger signal the relay drivers will switch off.

V_S	DC supply voltage / “jump start”	-0.3 to +28	V
	Single pulse / t_{max} < 400 ms “transient load dump”	-0.3 to +40	V
V_1	Stabilized supply voltage, logic supply	-0.3 to +5.25	V
V_2	Stabilized supply voltage	-0.3 to +28	V
V_{DI} V_{CLK} V_{TXD} V_{CSN} V_{DO} V_{RXD} V_{NRESET} V_{FSO} $V_{DIGOUT3,4}$	Logic input / output voltage range	-0.3 to V1+0.3	V
V_{INH} V_{PWM1}, V_{PWM2}, V_{REL1}, V_{REL2},	Wake up input voltage range PWM input voltage range Low side output voltage range	-0.3 to +40	V
$V_{OUT1..4,}$, V_{OUTH}	High side output voltage range	-0.3 to V_S + 0.3	V
$V_{WU1...4,}$	Wake up input voltage range	-0.3 to V_S + 0.3	V
$V_{OP1+,}$ $V_{OP1-,}$ $V_{OP2+,}$ $V_{OP2-,}$	Opamp1 input voltage range Opamp2 input voltage range	-0.3 to V1 + 0.3	V
$V_{OPOUT1,}$ V_{OPOUT2}	Analog Output voltage range	-0.3 to V_S + 0.3	V
$V_{LIN,}$ V_{LINPU}	LIN bus I/O voltage range	-20 to +40	V
I_{Input}	Current injection into Vs related input pins	5	mA

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit !

All pins, except LIN(1)	+/- 2	kV
All output pins(2)	+/- 4	kV
LIN(3)	+/- 1.5	kV
LIN(4)	+/- 8	kV
All pins (charge device model)	+/- 500	V
Corner pins (charge device model)	+/- 750	V
All pins(5)	+/- 200	V

1. HBM (human body model, 100pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A
2. HBM with all none zapped pins grounded
3. Without external components
4. Acc. DIN EN61000-4-2 (330Ω, 150pF), with external components:

- Diode, type ESDLIN1524BJ
- SMD Ferrite bead, type TDKMMZ2012Y202B
- Capacitor C=220pF

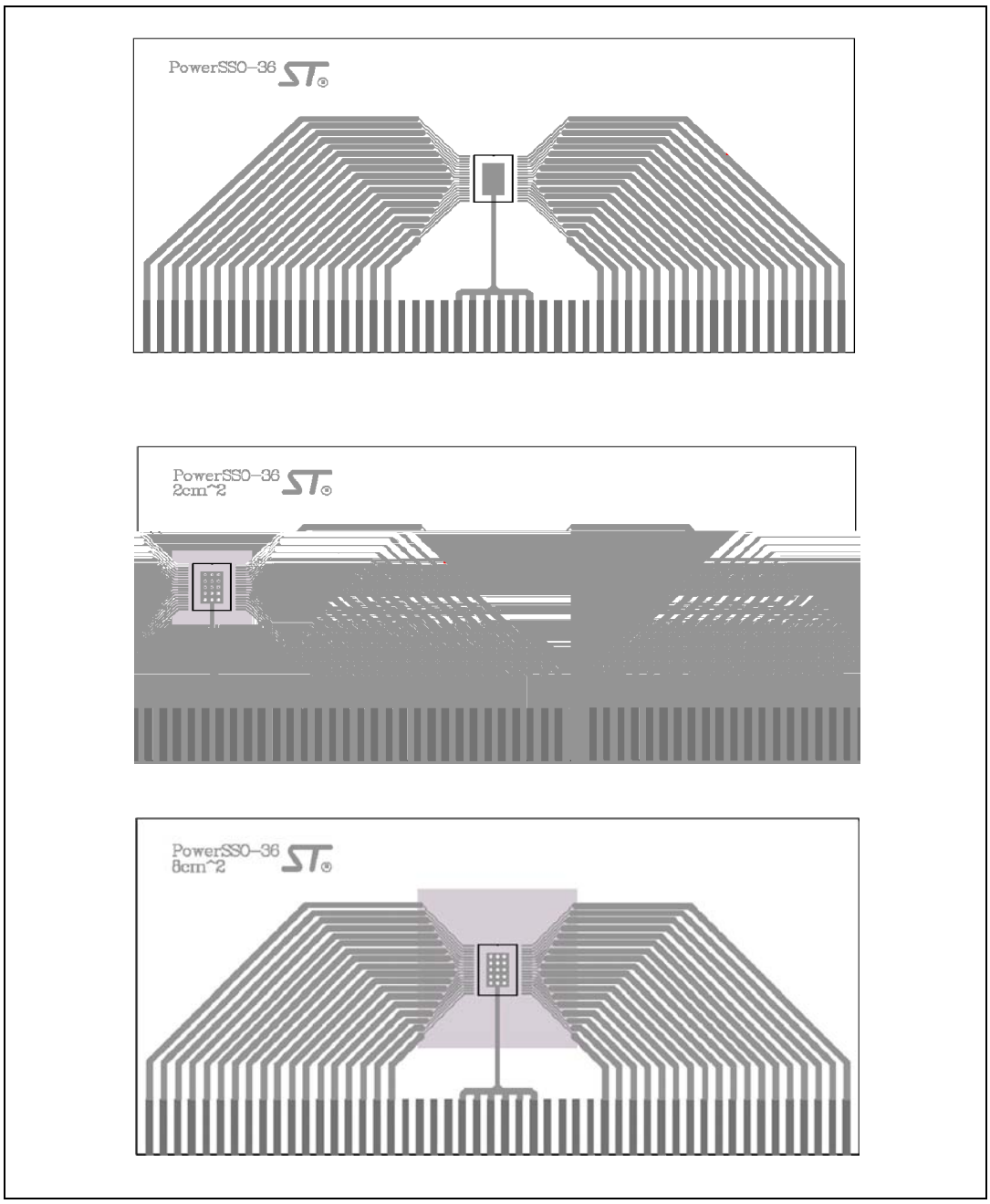
For detailed information please see EMC report from IBEE Zwickau (available on request)

5. Acc. Machine Model: C=220pF; L=0.75µH; R=10Ω

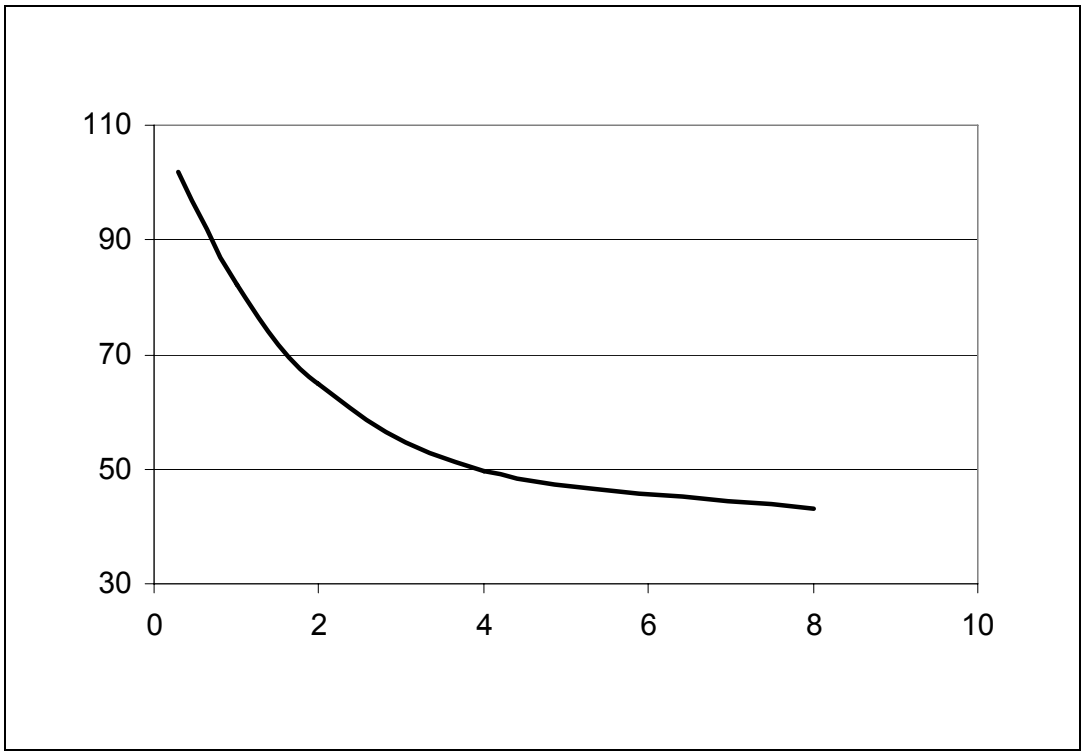
6.1.1	Tj	Operating junction temperature	- 40 to 150	°C
6.1.2	RthjA	Thermal resistance junction- ambient	See *Figure 10.*	°C/W

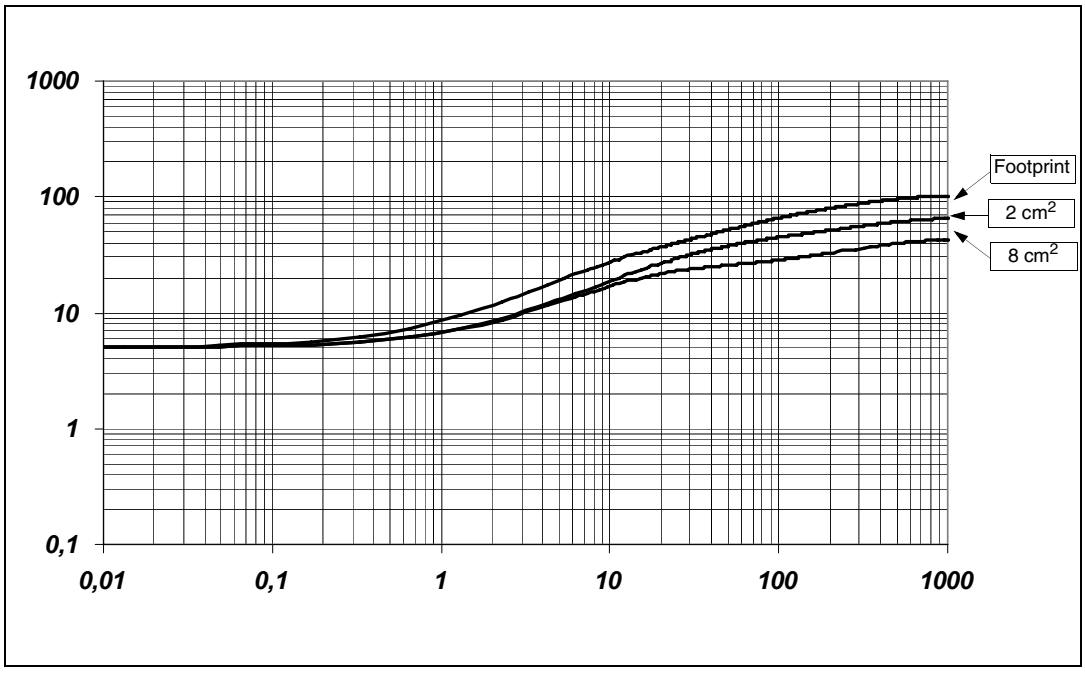
6.2.1	$T_{W\ ON}$	Thermal over temperature warning threshold	T_j (1)	120	130	140	°C
6.2.2	$T_{SD1\ OFF}$	Thermal shutdown junction temperature 1	T_j (1)	130	140	150	°C
6.2.3	T_{SD2OFF}	Thermal shutdown junction temperature 2	T_j (1)	140	155	170	°C
6.2.4	$T_{SD2\ ON}$		Hysteresis		5		°C
6.2.5	$T_{SD12hys}$						

1. Non-overlapping



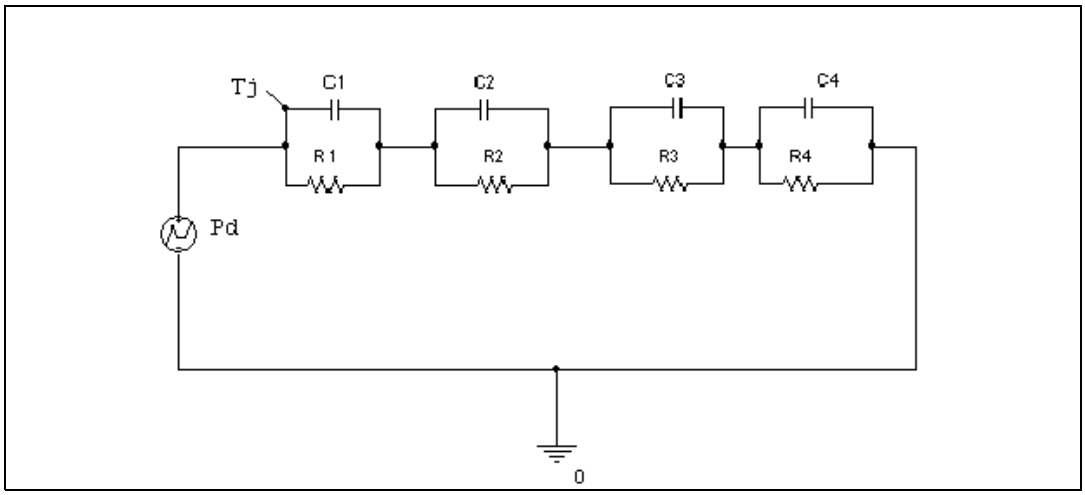
Note: Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10% board double layer, board dimension 129x60, board Material FR4, Cu thickness 0.070mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm).


110
90
70
50
30
0
2
4
6
8
10


1000
100
10
1
0,1
0,01
0,1
1
10
100
1000
Footprint
2 cm2
8 cm2

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$



R1 (°C/W)	5		
R2 (°C/W)	18	10	10
R3 (°C/W)	29	22	7,8
R4 (°C/W)	51	29	21
C1 (W.s/°C)	0,0003		
C2 (W.s/°C)	0,35	1	1
C3 (W.s/°C)	1,5	1,3	1,3
C4 (W.s/°C)	5	15	15

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.8V ≤ V1 ≤ 5.2V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.1.1	V_S	Supply voltage range		6	13.5	18	V
7.1.2	V_{SUV}	VS UV-threshold voltage	V_S increasing / decreasing	5.11		5.81	V
7.1.3	V_{hyst_UV}	Undervoltage hysteresis		0.04	0.1	0.15	V
7.1.4	V_{SOV}	VS OV-threshold voltage	V_S increasing / decreasing	18		22	V
7.1.5	V_{hyst_OV}	Overvoltage hysteresis	Hysteresis	0.5	1	1.5	V

6V ≤ V_S ≤ 18V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.2.1	F_{CLK}	Oscillation frequency	Vs = 6V...18V	0.808	1.01	1.35	MHz

All outputs open; T_j = - 40°C...130 °C, unless otherwise specified.

7.3.1	V_{THUP_POR}	V_{POR} threshold		2.8	3.45	4.1	V
7.3.2	V_{Hys_POR}	Hysteresis			200		mV

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 5.25V ≤ V_S ≤ 27V; T_j = -40°C...130°C, unless otherwise specified.

7.4.1	V1	Output voltage			5.0		V
7.4.2	V1	Output voltage tolerance Active mode	I_{LOAD} = 1mA... 100mA, VS = 13.5V			+/- 2	%
7.4.3	Vhc1	Output voltage tolerance Active mode, high current	I_{LOAD} = 100mA ... 250mA, VS = 13.5V			+/- 3	%
			I_{LOAD} = 250mA VS = 13.5V, T_j >80°C			+/- 4	%
7.4.4	VSTB1	Output voltage tolerance in low current mode	0mA≤ I_{LOAD}≤I_{CMP} VS = 13.5V			+/- 4	%
7.4.5	VDP1	Drop-out voltage in undervoltage conditions	I_{LOAD} = 50mA, V_S = 4.5V I_{LOAD} = 100mA, V_S =4.5V		0.2 0.3	0.4 0.5	V V
7.4.6	ICC1	Output current in active mode	Max. continuous load current			250	mA

7.4.7	ICCmax1	Short circuit output current	Current limitation	400	600	950	mA
7.4.8	Cload1	Load capacitor1	Ceramic(1)	0.22			µF
7.4.9	tTSD	V1 deactivation time after thermal shutdown			1		s
7.4.10	I_{CMP_ris}	Current comp. rising threshold	Rising current	0.9	2.5	4	mA
7.4.11	I_{CMP_fal}	Current comp. falling threshold	Falling current Tj= -40°C...130°C Tj= 25°C...130°C	 0.75 0.85	 1.95 1.95		mA
7.4.12	I_{CMP}_hys	Current comp. hysteresis			0.5		mA
7.4.13	V1fail	V1 fail threshold	V1 forced		2		V

1. Placement close to the PAD

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 5.25V ≤ V_S ≤ 27V; T_j = -40°C...130°C, unless otherwise specified.

7.5.1	V_2	Output voltage			5.0		V
7.5.2	V_2	Output voltage tolerance Active mode	I_{LOAD} = 1mA ... 50mA, V_S = 13.5V			+/- 3	%
7.5.3	V_{hc1}	Output voltage tolerance Active mode, high current	I_{LOAD} = 50mA ... 100mA, V_S = 13,5V			+/- 4	%
7.5.4	V_{STB2}	Output voltage tolerance in low current mode	I_{LOAD} = 0uA ...1mA V_S = 13,5V			+/- 5	%
7.5.5	V_{DP2}	Drop-out voltage	I_{LOAD} = 25mA, V_S = 5 V I_{LOAD} = 50mA, V_S= 5 V		0,3 0.4	0,4 0.7	V V
7.5.6	I_{CC2}	Output current in Active mode	Max. continuous load current			100	mA
7.5.7	I_{CCmax2}	Short circuit output current	Current limitation	200	300	500	mA
7.5.8	C_{load}	Load capacitor	Ceramic(1)	0.22			µF
7.5.9	$V2_{fail}$	V2 fail threshold	V2 forced			2	V

1. Placement close to the PAD

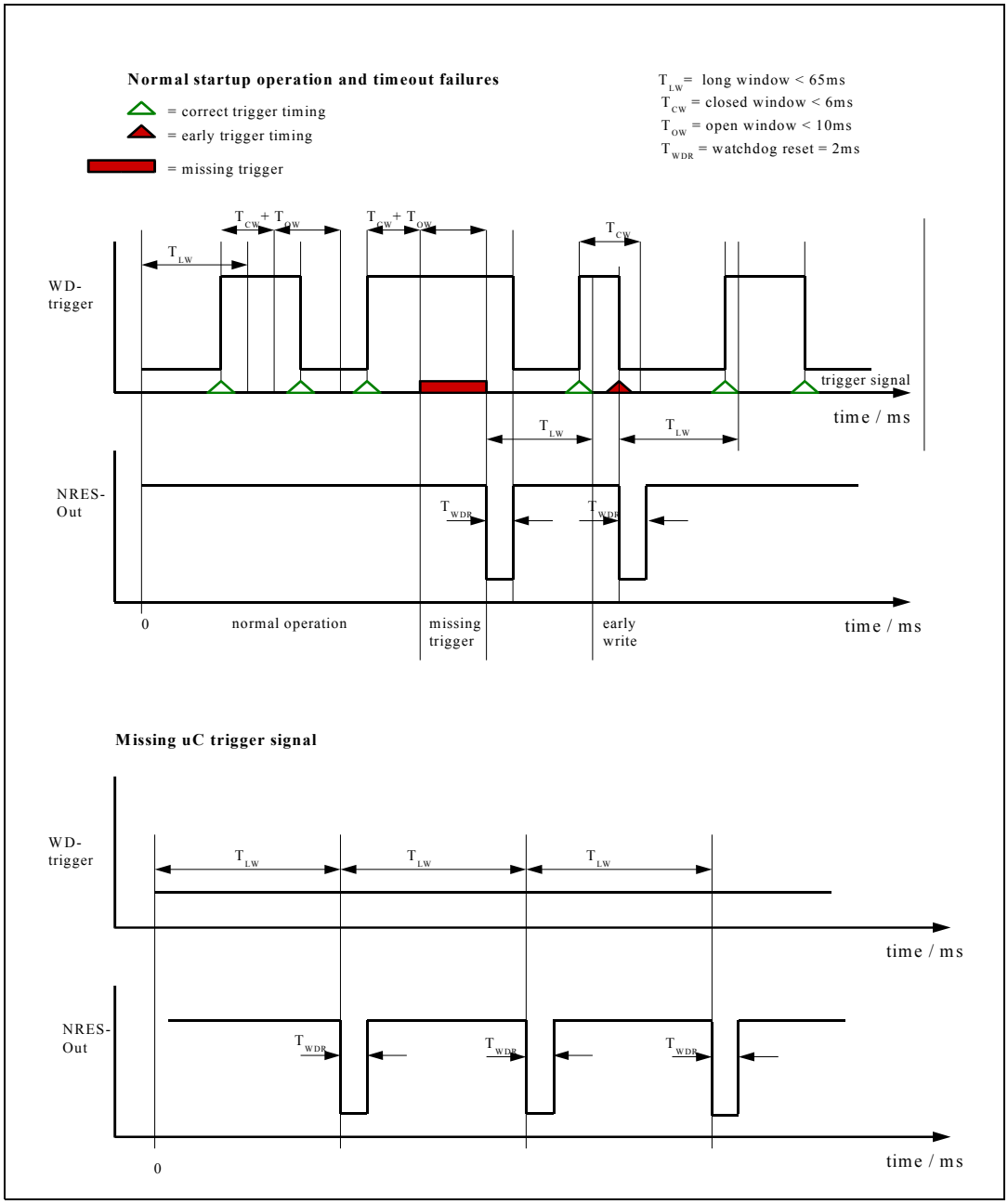
The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 5.25V < V_S = 18V; T_j = -40 to 130 °C, unless otherwise specified.

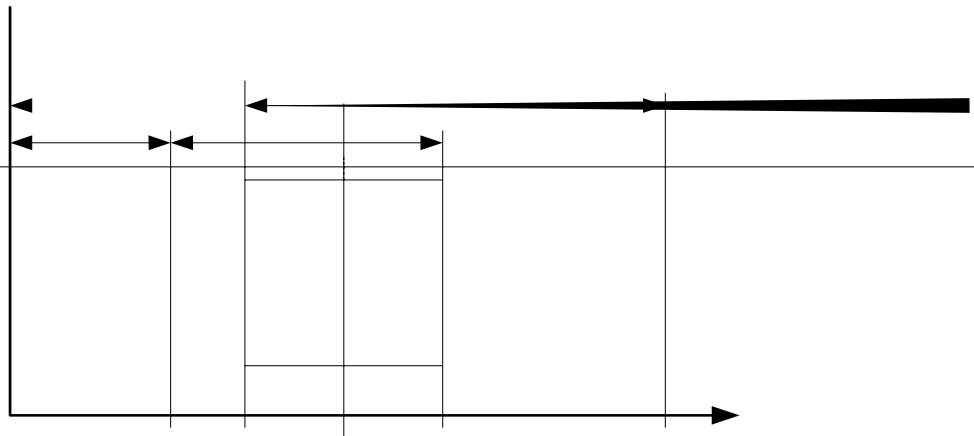
7.6.1	V_{RT1}	Reset threshold voltage1	V_S, V_{V1} inc. / decreasing	4.5	4.63	4.75	V
7.6.2	V_{RT2}	Reset threshold voltage2	V_S, V_{V1} inc. / decreasing	4.25	4.37	4.5	V
7.6.3	V_{RESET}	Reset pin low output voltage	V1 > 1V, I_{RESET} = 1mA		0,2	0,4	V
7.6.4	R_{RESET}	Reset pull up int. resistor		60	110	204	kΩ
7.6.5	t_{RR}	Reset reaction time	@Iload = 1mA	6		40	µs
7.6.6		V1 under-voltage filter time			16		µs

6V < V_S < 18V; 4.8V < V1 < 5.2V; T_j = -40 to 130 °C, unless otherwise specified

7.7.1	t_{LW}	Long open window		48,75	65	81,25	ms
7.7.2	t_{CW}	Closed window		4.5	6	7.5	ms
7.7.3	t_{OW}	Open window		7.5	10	12.5	ms
7.7.4	t_{WDR}	Watchdog reset pulse time		1.5	2	2. 5	ms

1. See *Figure 13*.


Normal startup operation and timeout failures
= correct trigger timing
= early trigger timing
= missing trigger
T LW = long window < 65ms
T CW = closed window < 6ms
T OW = open window < 10ms
T WDR = watchdog reset = 2ms
WD-trigger
NRES-Out
trigger signal
time / ms
0
normal operation
missing trigger
early write
Missing uC trigger signal



The voltages are referred to gnd and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.8V ≤ V1 ≤ 5.2V; T_j = -40°C...130°C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.8V ≤ V1 ≤ 5.2V; T_j = -40°C...130°C, unless otherwise specified.

7.8.11	R_{DSON}	On – resistance	I_{LOAD} = 60mA @ Tj=+25°C	0	7	12	Ω
7.8.12	I_{OUT}	Short circuit shutdown current	8V < Vs < 16V	140	235	330	mA
7.8.13	I_{OLD1}	Open load detection current 1	Selectable via SPI	0.8	2	4	mA
7.8.14	I_{OLD2}	Open load detection current 2		6	8	13	mA
7.8.15	SR	Slew rate		0.2	0.5	0.8	V/µs
7.8.16	t_{dONHS}	Switch ON delay time	0.2 V_S	10	35	60	µs
7.8.17	t_{dOFFHS}	Switch OFF delay time	0.8 V_S	40	95	150	µs
7.8.18	t_{SCF}	Short circuit filter time	Tested by scan chain		64* T_{OSC}		
7.8.19	I_{FW} (1)	Loss of GND current (ESD structure)		100			mA

1. Parameter guaranteed by design

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.8V ≤ V1 ≤ 5.2V; T_j = -40 to 130 °C, unless otherwise specified.

7.9.1	R_{DSON}	DC output resistance	ILOAD = 100mA @ Tj = +25°C	0	2	3	Ω
7.9.2	I_{OUT}	Short circuit shutdown current	8V < Vs < 16V	250	375	500	mA
7.9.3	V_Z	Output clamp voltage (1)	I_{LOAD} = 100mA	40		48	V
7.9.4	t_{ONHL}	Turn on delay time to 10% V_{OUT}		5	50	100	µs
7.9.5	t_{OFFLH}	Turn off delay time to 90% V_{OUT}		5	50	100	µs

7.9.6	t_{SCF}	Short circuit filter time	Tested by scan chain		64* T_{OSC}		
7.9.7	SR	Slew Rate		0.2	2	4	V/µs

1. The output is capable to switch off relay coils with the impedance of RL=160Ω; L = 300mH (RL=220Ω; L= 420mH); at V_S = 40V (Load dump condition)

..

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; T_j = -40 to 130 °C, unless otherwise specified.

7.10.1	V_{WUthp}	Wake-up negative edge threshold voltage		0.4 Vs	0.45 Vs	0.5 Vs	V
7.10.2	V_{WUthn}	Wake-up positive edge threshold voltage		0.5 Vs	0.55 Vs	0.6 Vs	V
7.10.3	V_{HYST}	Hysteresis		0.05 Vs	0.1 Vs	0.15 Vs	V
7.10.4	t_{WU}	Minimum time for wake-up		51	64	77	µs
7.10.5	I_{WU_stdby}	Input current in standby mode	1.5V<V_{IN}< (Vs-3V)	10	20	30	µA
7.10.6	R_{WU_act}	Input resistor to GND in active mode and in standby mode during wake-up request		100	275	450	kΩ
7.10.7	Nn	Number of samples	During OUT_HS on, cyclic sense mode (100us cyclic HS on time)	2 (at 80µs and 100µs)			
7.10.8	V_{wuthl}	Pending wake up request low threshold		1.0	1.25	1.5	V
7.10.9	V_{wuthh}	Pending wake up request high threshold		Vs-3	Vs-2.2	Vs-1.4	V

1. Defines whether the inputs W1..4 are configured with current source or current sink in standby mode.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; T_j = -40 to 130 °C, unless otherwise specified.

7.11.1	I_{INHth}	Wake-up activate threshold current		30	75	120	µA
7.11.2	I_{INHUth}	Wake-up passive threshold current		30	70	120	µA
7.11.3	I_{INHhys}	Wake-up current hysteresis			10	20	µA
7.11.4	t_{WU}	Minimum time for wake-up		51	64	77	µs
7.11.5	Nn	Number of samples	During OUT_HS on, cyclic sense mode (100µs cyclic HS on time)	2 (at 80us and 100us)			

Compatible to Lin 2.1 for Baud rates up to 20 kBit/s

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6V ≤ V_S ≤ 18V; 4.8V ≤ V1 ≤ 5.2V; T_j = -40°C...130°C, unless otherwise specified.

7.12.1	V_{TXDLOW}	Input voltage dominant level	Normal mode, V1=5V	1	1.3		V
7.12.2	$V_{TXDHIGH}$	Input voltage recessive level	Normal mode, V1=5V		2.2	2.5	V
7.12.3	V_{TXDHYS}	$V_{TXDHIGH}$ - V_{TXDLOW}	Normal mode, V1=5V	0.5	0.8		V
7.12.4	I_{TXDPU}	TXD pull up current	Normal and V1-standby mode , V1=5V	-5	-30	-60	µA
7.12.5	I_{TXDPD}	TXD pull-down current	V_{BAT} - standby mode, $V_{TXDHIGH}$ V1=5V	5	30	60	µA
7.12.6	V_{RXDLOW}	Output voltage dominant level	Normal mode, V1=5V, 2mA		0.2	1.5	V

7.12.7	$V_{RXDHIGH}$	Output voltage recessive level	Normal mode, V1=5V, 2mA	4.5			V
7.12.8	V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4 V_S	0.45 V_S	0.5 V_S	V
7.12.9	V_{THrec}	Receiver threshold voltage dominant to recessive state		0.5 V_S	0.55 V_S	0.6 V_S	V
7.12.10	V_{THhys}	Receiver threshold hysteresis	V_{THrec} - V_{THdom}	0.07 V_S	0.1 V_S	0.175 V_S	V
7.12.11	V_{THcnt}	Receiver tolerance center value	(V_{THrec} + V_{THdom}) / 2	0.475 V_S	0.5 V_S	0.525 V_S	V
7.12.12	V_{THwkup}	Receiver wakeup threshold voltage		1.0	1.5	2	V
7.12.13	$V_{THwkdwn}$	Receiver wakeup threshold voltage		3.5 Vs	2.5 Vs	1.5 Vs	V
7.12.14	Tbus	Dominant time for wakeup via bus	Sleep mode edge: rez.- dom.		64		µs

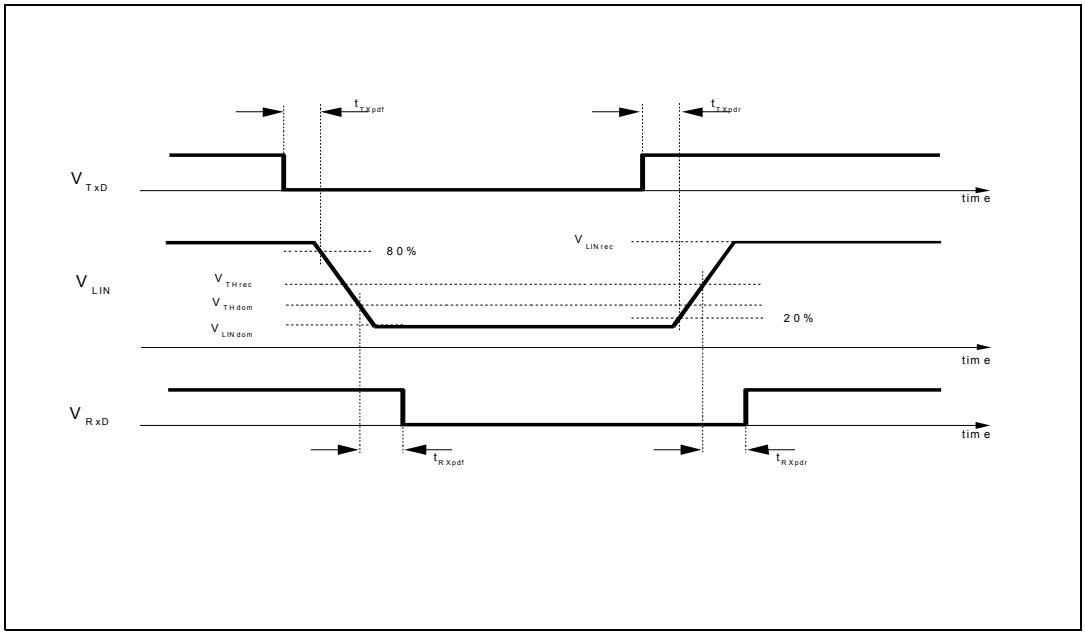
7.12.15	$I_{LINDomSC}$	Transmitter input current limit in dominant state	V_{TxD} = V_{TxDlow} V_{LIN} = Vbatmax = 18V	40	100	180	mA
7.12.16	$I_{bus\_PAS\_dom}$	Input leakage current at the receiver incl. Pull-Up resistor	V_{TxD} = $V_{TxDhigh}$ V_{LIN} = 0V, V_{BAT} =12V, Slave mode	-1			mA
7.12.17	$I_{bus\_PAS\_drec}$	Transmitter input current in recessive state	V_{TxD} = $V_{TxDhigh}$ 8V<V_{LIN}, V_{BAT}<18V; $V_{LIN} \geq V_{BAT}$			20	µA
7.12.18	$I_{bus\_NO\_GND}$	Input current if loss of GND at Device	GND = Vs, 0V<V_{LIN}<18V V_{BAT}=12V	-1		1	mA
7.12.19	I_{bus}	Input current if loss of Vbat at device	GND = Vs, 0V<V_{LIN}<18V			100	µA

7.12.20	V_{LINdom}	LIN voltage level in dominant state	$V_{TxD} = V_{TxDlow}$ I_{LIN} = 40mA			1.2	V
7.12.21	V_{LINrec}	LIN voltage level in recessive state	$V_{TxD} = V_{TxDhigh}$ I_{LIN} = 10µA	0.8 Vs			V
7.12.22	R_{LINup}	LIN output pull up resistor	V_{LIN} = 0V	20	40	60	kΩ

7.12.24	t_{TXpd_sym}	Symmetry of transmitter propagation delay time (rising vs. falling edge)	tTXpd_sym = = tTXpdr – tTXpdf Vs=12V, Rbus Cbus: 1 kΩ, 1 nF	-2.5	-	2.5	µs
7.12.25	t_{RXpd}	Receiver propagation delay time	tRXpd = = max (tRXpdr tRXpdf) tRXpdf = =t(0.5RXD)-t(0.45 VLin) tRXpdr = =t(0.5RXD)-t(0.55 VLin) Crxd = 20pF Vs = 12V, Rbus Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω,10 nF		-	6	µs
7.12.26	tRXpd_sym	Symmetry of receiver propagation delay time (rising vs. falling edge)	tRXpd_sym = = tRXpdr – tRXpdf	-2	-	2	µs

7.12.27	D1	Duty cycle 1	THRec(max)=0.744*Vs THDom(max)=0.581*Vs Vs= 7...18V, tbit= 50us, D1=tbus_rec(min)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF	0.396	-		
7.12.28	D2	Duty cycle 2	THRec(min)=0.284*Vs; THDom(min)=0.422*Vs, Vs= 7.6 ...18V, tbit= 50µs, D1=tbus_rec(max)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF		-	0.581	
7.12.29	D3	Duty cycle 3	THRec(max)=0.778*Vs; THDom(max)=0.616*V, Vs= 7...18V tbit= 96µs, D3 =tbus_rec(min)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF	0.417	-		
7.12.30	D4	Duty cycle 4	THRec(min)=0.251*Vs; THDom(min)=0.389*Vs, Vs= 7.6 ...18V, tbit= 96µs D1 =tbus_rec(max)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω,10 nF		-	0.59	

7.12.31	R_{DSon}	ON resistance			10.5	16	Ω
7.12.32	I_{leak}	Leakage current				1	uA


t TXpdf
t TXpdr
V TxD
time
V LIN
80 %
V LINrec
V THrec
V THdom
V LINdom
20 %
time
V RxD
time
t RXpdf
t RXpdr

The voltages are referred to gnd and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; T_j = -40...130°C, unless otherwise specified.

7.13.1	GBW	GBW product		1	3.5	7.0	MHz
7.13.2	$AVOL_{DC}$	DC open loop gain		80			dB
7.13.3	PSRR	Power supply rejection	DC, Vin =150 mV	80			dB
7.13.4	V_{off}	Input offset voltage		-5		+5	mV
7.13.5	V_{ICR}	Common mode input range		-0.2	0	3	V
7.13.6	V_{OH}	Output voltage range high	Iload = 1mA to Gnd	0.2 V_S		V_S	V
7.13.7	V_{OL}	Output voltage range low	Iload = 1mA to V_S	0		0.2	V
7.13.8	I_{lim+}	Output current limitation +	DC	5	10	20	mA
7.13.9	I_{lim-}	Output current limitation -	DC	-5	-10	-20	mA
7.13.10	SR+	Slew rate positive		1	4	10	V/µs
7.13.11	SR-	Slew rate negative		-1	-4	-10	V/µs

Note: The operational amplifier is on-chip stabilized for external capacitive loads C_L ≤ 25pF (all operating conditions)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.5V ≤ V1 ≤ 5.3V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.1	V_{CSNLOW}	Input voltage low level	Active mode, V1 = 5V	0.5	1.0	1.6	V
7.14.2	$V_{CSNHIGH}$	Input voltage high level	Active mode, V1=5V	1	1.75	2.5	V
7.14.3	V_{CSNHYS}	VCSNHIGH - VCSNLOW	Active mode, V1=5V	0.5	1.0	1.5	V
7.14.4	I_{CSNPU}	CSN pull up current	Active mode and V1 Standby mode,V1=5V	-5	-30	-60	µA
7.14.5	I_{CSNPD}	CSN pull-down current	In V_{bat}- standby mode	5	30	60	µA

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V≤ V_S ≤18V; 4.5V ≤ V1 ≤ 5.3V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.6	t_{set}	Delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	µs
7.14.7	$V_{in\ L}$	Input low level	V1 = 5 V	1.0	2.05	2.5	V
7.14.8	$V_{in\ H}$	Input high level	V1 = 5 V	1.5	2.8	3.3	V
7.14.9	$V_{in\ Hyst}$	Input hysteresis	V1 = 5 V	0.4	0.75	1.5	V
7.14.10	I_{in}	Pull down current at input	V_{in} = 1.5 V	5	30	60	µA
7.14.11	C_{in}(1)	Input capacitance at input CSN, CLK, DI and $PWM_{1,2}$	0V < V1 < 5.3V		10	15	pF
7.14.12	f_{CLK}	SPI input frequency at CLK				1	MHz

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

The voltages are referred to ground.

$6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.13	$V_{in\ L}$	Input low level (Vin rising))	V1 = 5 V	6.1	7.25	8.4	V
7.14.14	$V_{in\ H}$	Input high level (Vin falling)	V1 = 5 V	7.4	8.4	9.4	V
7.14.15	$V_{in\ Hyst}$	Input hysteresis	V1 = 5 V	0.6	0.8	1.0	V

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.16	t_{CLK}	Clock period	V1 = 5 V	1000	-		ns
7.14.17	t_{CLKH}	Clock high time	V1 = 5 V	400	-		ns
7.14.18	t_{CLKL}	Clock low time	V1 = 5 V	400	-		ns
7.14.19	$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V1 = 5 V	400	-		ns
7.14.20	$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V1 = 5 V	400	-		ns
7.14.21	$t_{set\ DI}$	DI setup time	V1 = 5 V	200	-		ns
7.14.22	$t_{hold\ DI}$	DI hold time	V1 = 5 V	200	-		ns
7.14.23	t_{r_in}	Rise time of input signal DI, CLK, CSN	V1 = 5 V		-	100	ns
7.14.24	t_{f_in}	Fall time of input signal DI, CLK, CSN	V1 = 5 V		-	100	ns

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.5V ≤ V1 ≤ 5.3V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.25	V_{DOL}	Output low level	V1 = 5 V, I_D = -4mA			0.5	V
7.14.26	V_{DOH}	Output high level	V = 5 V, I_D = 4 mA	4.5			V
7.14.27	I_{DOLK}(1)	Tristate leakage current	V_{CSN} = V1, 0 V < V_{DO} < V1	-10		10	uA
7.14.28	C_{DO}	Tristate input capacitance	V_{CSN} = V1, 0 V < V1 < 5.3 V		10	15	pF

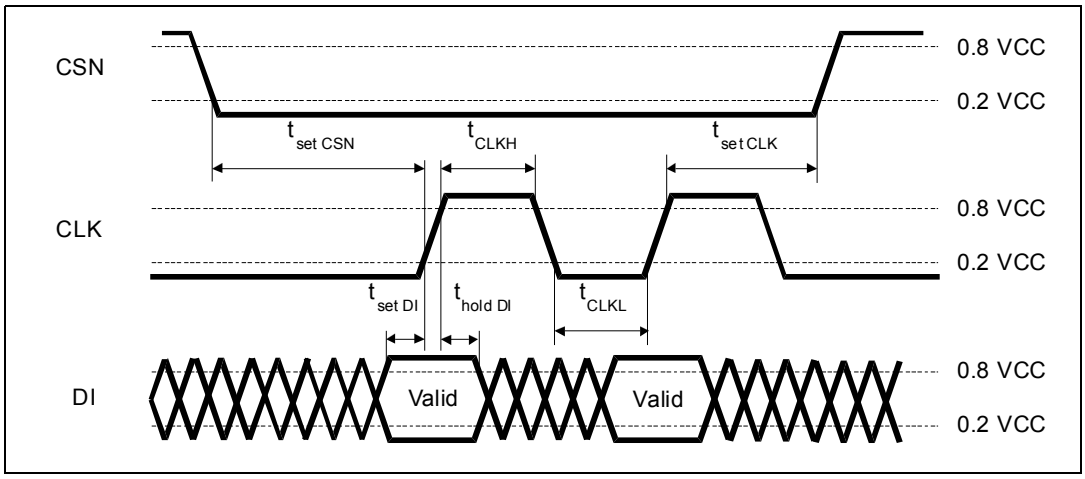
1. Not valid for FSO

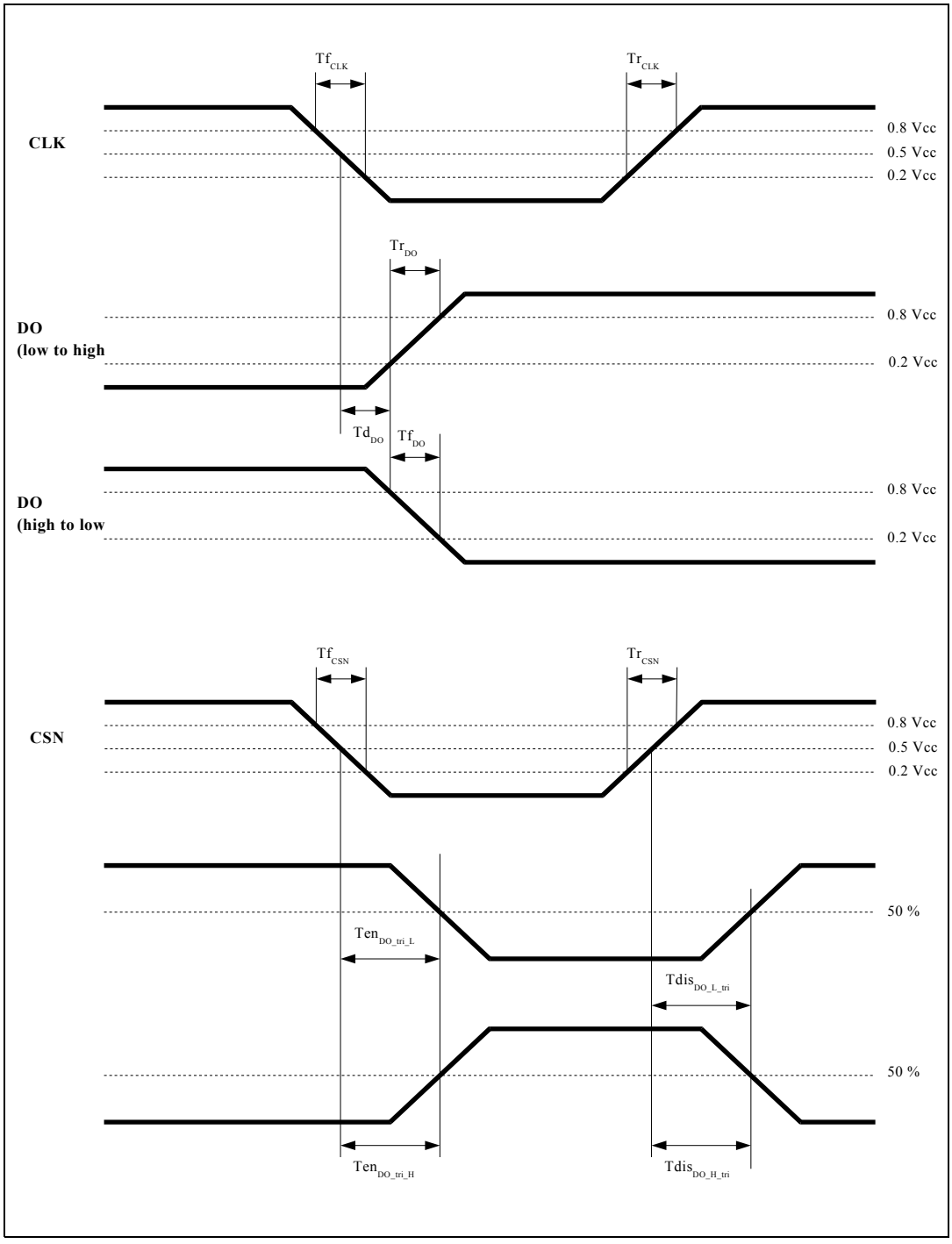
The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.5V ≤ V1 ≤ 5.3V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

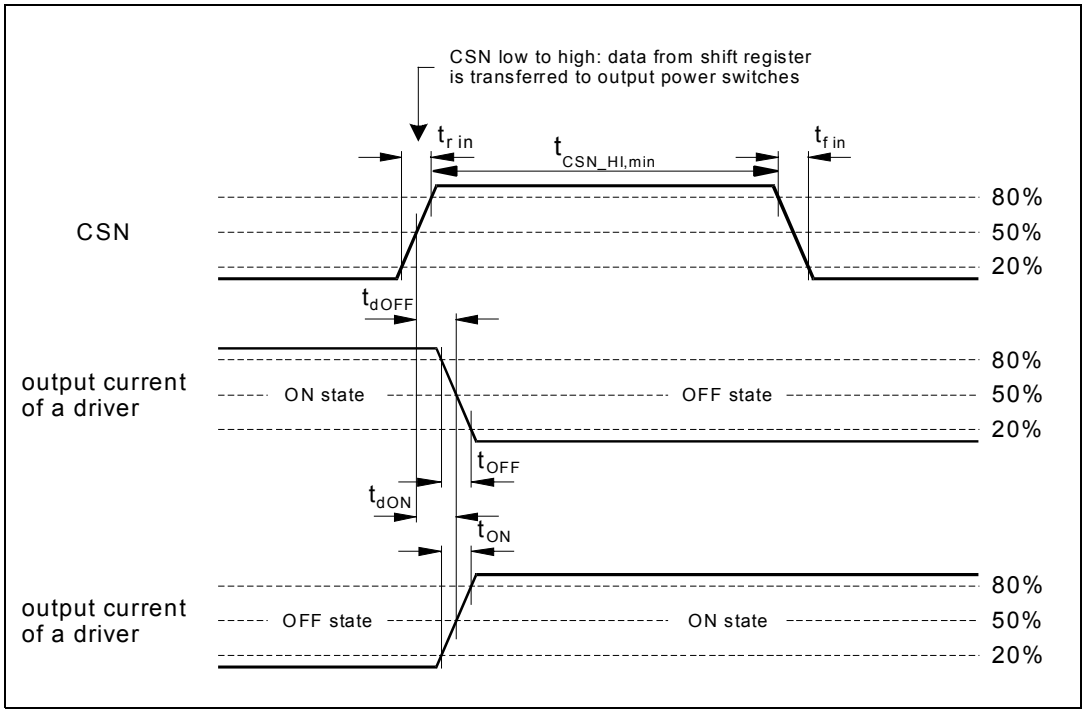
7.14.29	$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1 mA	-	50	100	ns
7.14.30	$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1 mA	-	50	100	ns
7.14.31	$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_L = 100 pF, I_{load} = 1 mA pull-up load to V1	-	50	250	ns
7.14.32	$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_L = 100 pF, I_{load} = 4 mA pull-up load to V1	-	50	250	ns
7.14.33	$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_L = 100 pF, I_{load} = -1 mA pull- down load to GND	-	50	250	ns
7.14.34	$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_L = 100 pF, I_{load} = -4 mA pull-down load to GND	-	50	250	ns
7.14.35	$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V1, V_{DO} > 0.7 V1, C_L = 100 pF	-	50	250	ns

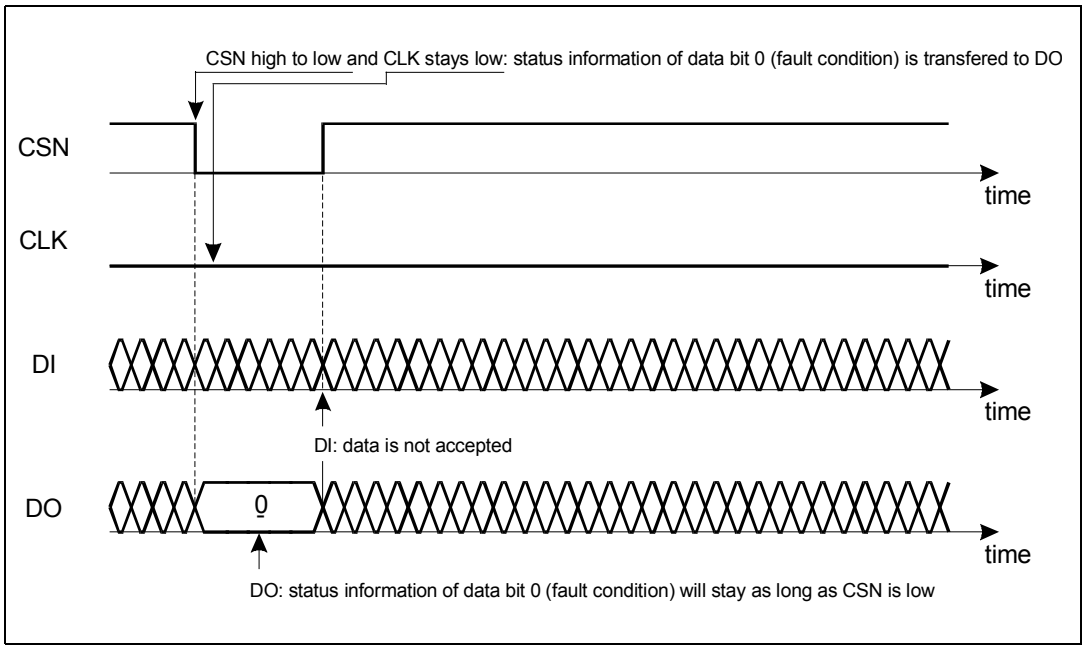
The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18V; 4.5V ≤ V1 ≤ 5.3V; all outputs open; T_j = -40°C...130°C, unless otherwise specified.

7.14.36	$t_{CSN\_HI,min}$	Minimum CSN HI time, active mode	Transfer of SPI-command to input register	6	-	-	µs




Tf_CLK
Tr_CLK
CLK
0.8 Vcc
0.5 Vcc
0.2 Vcc
Tr_DO
DO
(low to high
0.8 Vcc
0.2 Vcc
Td_DO
Tf_DO
DO
(high to low
0.8 Vcc
0.2 Vcc
Tf_CSN
Tr_CSN
CSN
0.8 Vcc
0.5 Vcc
0.2 Vcc
50 %
Ten_DO_tri_L
Tdis_DO_L_tri
50 %
Ten_DO_tri_H
Tdis_DO_H_tri


CSN low to high: data from shift register
is transferred to output power switches
$t_{r\ in}$
$t_{CSN\_HI,min}$
$t_{f\ in}$
CSN
80%
50%
20%
t_{dOFF}
output current
of a driver
ON state
OFF state
80%
50%
20%
t_{OFF}
t_{dON}
t_{ON}
output current
of a driver
OFF state
ON state
80%
50%
20%


CSN high to low and CLK stays low: status information of data bit 0 (fault condition) is transfered to DO
CSN
time
CLK
time
DI
time
DI: data is not accepted
DO
0
time
DO: status information of data bit 0 (fault condition) will stay as long as CSN is low

24bit shift register: first 2 bits are address (A1,A0) and 22 bits are data.

During power-on reset, all registers are set to zero.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A1	A0	Data																					
Address																							
[write]					On5V2		On Signals																
Control Register 0		GO VCC	GO V_{BAT}	TRIG	ON V21	ON V20	REL 2	REL 1	OUT HS2	OUT HS1	OUT HS0	HS 42	HS 41	HS 40	HS 32	HS 31	HS 30	HS 22	HS 21	HS 20	HS 12	HS 11	HS 10
0	0	Address																					
[write]				Timer 2	Timer 1				Loop			Pullup / down				Wakeup Sources OL				Wakeup Sources			
Control Register 1		CLR	INT_en	T20	T13	T12	T11	T10	L2	L1	L0	U3	U2	U1	U0	W7	W6	W5	W4	W3	W2	W1	W0
0	1	Address																					
[write]					Input config									Reset level		LIN				Openload treshold			
Control Register 2		RES	I_{CMP}	LS OVUV	LIN Slope	IC 41	IC 40	IC 31	IC 30	IC 21	IC 20	IC 11	IC 10	LEV 1	LEV 0	TXT TOUT	LINPU	O_HS REC	VLOCK OUT	OLT HS4	OLT HS3	OLT HS2	OLT HS1
1	0	Address																					
[read]		Reserved		Wakeup			Wakeup input status				Overcurrent								Openload				
Status Register 0		RES	RES	COLD START	LIN	INH	WU4	WU3	WU2	WU1	SHT5 V2	Rel2 OC	Rel1 OC	HS OC	HS4 OC	HS3 OC	HS2 OC	HS1 OC	HS OL	HS4 OL	HS3 OL	HS2 OL	HS1 OL
Err	Err	Address																					
		Reserved		LIN State				Watchdog Reset				5V Restarts			State								
Status Register 1		RES	RES	DOM TXD	SHT BAT	SHT GND	TRIG	WD 3	WD 2	WD 1	WD 0	R2	R1	R0	ST1	ST0	VCC_2 Fail	VCC_1 Fail	TSD 2	TSD 1	TW	UV	OV
Err	Err	Address																					

Note: During the shift in of the address bits, (2 clock periods) an internal error bit (Err) is fed to the DO output.

D23,D22 -> error flags (seen from DO)

The error flag is generated by logic OR combination of following error bits:

VCC_Fail1,2; TSD1,2; TW; OV,UW; OC_HS1..4; OC_OUTHS; OC_REL1..2; OC_V2

While writing to the control register 0, the status register 0 can be read at the DO-Output of the SPI.

	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GO V1	GO V_{bat}	TRIG	ON V21	ON V20	REL 2	REL 1	OUT HS2	OUT HS1	OUT HS0	HS 42	HS 41	HS 40	HS 32	HS 31	HS 30	HS 22	HS 21	HS 20	HS 12	HS 11	HS 10

HSx2	HSx1	HSx0	Defines the output configuration of the High Side Drivers 1-4

OUT_HS 2	OUT_HS 1	OUT_HS 0	Defines the output configuration of the High Side Driver OUT_HS
0	0	0	Driver is OFF in all modes
0	0	1	Driver is ON in active mode, off in standby mode
0	1	0	Driver is cyclic ON with the timing of Timer 1 in active mode and standby modes
0	1	1	Driver is cyclic ON with the timing of Timer 2 in active mode and standby modes
1	0	0	Driver is controlled by the PWM1 Input
1	0	1	Driver is controlled by the PWM2 Input

RELx	Defines the Output configuration of the low side relay drivers 1/2
0	Driver is OFF in all modes
1	Driver is ON in active mode (off in standby mode)

On_V21	On_V20	Defines in which modes the voltage regulator 2 is on
0	0	Voltage regulator 2 is OFF in all modes

0	1	Voltage regulator 2 is ON in ACTIVE mode; OFF in V_1-standby, V_{Bat}-standby
1	0	Voltage regulator 2 is ON in ACTIVE mode and V_1 standby; OFF in V_{bat}-standby
1	1	Voltage regulator 2 is ON in all modes

TRIG	Trigger bit for watchdog; inverted for each Trigger event invert this bit for a proper watchdog trigger.
GO_VBAT	”1” enters the V_{bat}-standby mode. (dominant mode, if both standby modes are selected)
GO_V1	“1” enters the V_1-standby mode.

While writing to the control register 1, the status register 1 can be read at the DO-Output of the SPI.

	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CLR	INT_EN	T20	T13	T12	T11	T10	L2	L1	L0	U3	U2	U1	U0	W7	W6	W5	W4	W3	W2	W1	W0

W7	W6	W5	W4	W3	W2	W1	W0	Disables the corresponding wake up sources
x	x	x	x	x	x	x	1	Input WU1 is disabled as wake up source
x	x	x	x	x	x	1	x	Input WU2 is disabled as wake up source
x	x	x	x	x	1	x	x	Input WU3 is disabled as wake up source
x	x	x	x	1	x	x	x	Input WU4 is disabled as wake up source
x	x	x	1	x	x	x	x	Open load Appearance / Disappearance at OUT1 is disabled as wake up source
x	x	1	x	x	x	x	x	Open load Appearance / Disappearance at OUT2 is disabled as wake up source
x	1	x	x	x	x	x	x	Open load Appearance / Disappearance at OUT3 is disabled as wake up source

1	x	x	x	x	x	x	x	Open load Appearance / Disappearance at OUT4 is disabled as wake up source
0	0	0	0	0	0	0	0	Default: all wake up sources are enabled

U3	U2	U1	U0	Defines whether the Inputs WU1..4 are configured with current source or current sink in standby mode.
x	x	x	1	Input WU1 configured with a current source in standby mode (R_{WU_act} pulldown resistor in active mode - see *Table 20.*)
x	x	1	x	Input WU2 configured with a current source in standby mode (R_{WU_act} pulldown resistor in active mode - see *Table 20.*)
x	1	x	x	Input WU3 configured with a current source in standby mode (R_{WU_act} pulldown resistor in active mode - see *Table 20.*)
1	x	x	x	Input WU4 configured with a current source in standby mode (R_{WU_act} pulldown resistor in active mode - see *Table 20.*)
0	0	0	0	Default: All Inputs configured with a current sink in standby (R_{WU_act} pulldown resistor in active mode - see *Table 20.*)

L2	L1	L0	Defines which signal is looped to the Dig_Out3 and Dig_Out4 (see note)	
			Dig_Out3	Dig_Out4
0	0	0	WU3 (default)	WU4 (default)
0	0	1	HighZ	WU4
0	1	0	WU3	HighZ
0	1	1	WU3	Open Load HS2
1	0	0	Open Load HS1	WU4
1	0	1	Open Load HS1	Open Load HS2
1	1	0	Open Load HS1	HighZ
1	1	1	HighZ	Open Load HS2

T12	T11	T10	Defines the period of the cyclic sense Timer 1 which is selectable for Out 1..4 and Out_HS (see ON signals control register 0)
0	0	0	Period: 0.5 s
0	0	1	Period: 1.0 s
0	1	0	Period: 1.5 s
0	1	1	Period: 2.0 s
1	0	0	Period: 2.5 s
1	0	1	Period: 3.0 s
1	1	0	Period: 3.5 s
1	1	1	Period: 4.0 s
T13			Defines the ON time for the cyclic sense Timer1
0			ON time 10 ms
1			ON time 20 ms
T20			Defines the ON time of the cyclic sense Timer 2 which is selectable for Out 1..4 and OUTHS (see ON Signals control register 0)
0			Period 50 ms / ON time 100 us
1			Period 50 ms / ON time 1ms

INT_enable	
0	Interrupt Mode disabled (see *Section 2.7*)
1	Interrupt Mode enabled
CLR	Clears the contents of status register 0 and 1

Note: In V_{BAT} standby mode, DigOut 3 and DigOut4 are HighZ.

While writing to the control register 2, the status register 0 can be read at the DO-Output of the SPI.

					Input filter configuration																	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	W		W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RES	I_{CMP}	LSO VUV	LIN Slope	IC 41	IC 40	IC 31	IC 30	IC 21	IC 20	IC 11	IC 10	LEV 1	LEV 0	TXDT Out	LINP U	O_HS REC	VS Lock Out	OLT HS4	OLT HS3	OLT HS2	OLT HS1

OLT_HSx	Open load threshold for the High Side Drivers Out1..4 0: Iopenload = 2mA; 1: Iopenload = 8mA
VSLOCK Out	Automatic recovery after VS Over/Under voltage “0” (default): Vs lockout is disabled, i.e. outputs will automatically recover (according to output settings in CR0) after Vs over / under - voltage conditions has disappeared “1”: Vs lockout is enabled, i.e. outputs will remain Off after Vs over / under voltage recovery conditions has disappeared, until the Vs over / under voltage Status Bits (SR1, bit s0,1) are cleared by CLR command (CR1, bit 21).
O_HS_REC	“1” = Recovery mode for OUT_HS Driver.
LINPU	“1” will disable the master pull up LINPU
TXD_TOUT	“1” will disable the dominant TxD time-out for the LIN Interface.

LEV1	LEV0	Controls the reset level
0	0	Set the reset threshold to 4.65V, typ.
0	1	Set the reset threshold to 4.35V, typ.
1	X	Reserved (do not use for operation, set LEV1 to “0”)

IC(1..4)1		IC(1..4)0	Selects the filter configuration for the Wakeup Inputs WU1 to 4
IC11	0	0	Filter with 64 us Filter time (static sense)
IC21	0	1	Enable Filter after 80 us with a Filter time of 16 us (cyclic sensing), timer2
IC31	1	0	Enable Filter after 800 us with a Filter time of 16 us (cyclic sensing), timer2
IC41	1	1	Enable Filter after 800 us with a Filter time of 16 us (cyclic sensing), timer1

LIN slope	Change LIN slope
0	High slew rate (default)
1	Low slew rate
LS_ovuv	Vs Over / Under voltage shutdown of REL1,2 (low side drivers)
0	Enable (default): REL1,2 turned Off in case of Vs Over/Undervoltage
1	Disable : REL1,2 remain On in case of Vs Over/Undervoltage
I_{CMP}	Current supervision of V1 regulator in V_1-standby mode.
0	Enable (default)
1	Disable
RES	Reserved

The contents of the status register 0 can be read implicitly, while accessing the control register 0 or control register 2.

	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RES	RES	Cold Start	LIN	INH	WU 4	WU 3	WU 2	WU 1	SHT5V2	REL 2OC	REL 1OC	HS OC	HS 4OC	HS 3OC	HS 2OC	HS 10C	HS O L	HS 4OL	HS 3OL	HS 2OL	HS 1OL

HS1..4_OL	Open load status from the High Side Driver OUT1..4.
0	No open load has been detected.
1	Open load has been detected.
HS_OL	Open load status from the High Side Driver OUT_HS
0	No open load has been detected.
1	Open load has been detected.
HS1..4_OC	Over current status from the High Side Driver OUT1..4.
0	No over current has been detected.
1	Over current has been detected.
HS_OC	Over current status from the High Side Driver OUT_HS.
0	No over current has been detected.
1	Over current has been detected.
Rel 1,2_OC	Over current status from Relais1,2
0	No over current has been detected.
1	Over current has been detected.

INH	Wakeup initiated through INH source
LIN	Wakeup initiated through LIN source
Cold Start	Set to high when the internal Power on Reset occurs. Will be cleared with the first SPI access.

Note: RES = reserved bits.

The contents of the status register 1 can be read implicitly, while accessing the control register 1.

	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RES	RES	DOM TXD	SHT BAT	SHT GND	TRIG	WD 3	WD 2	WD 1	WD 0	R2	R1	R0	ST1	ST0	V2 Fail	V1 Fail	TSD 2	TSD 1	TW	UV	OV

OV Over voltage failure of Vs.

UV Under voltage failure of Vs.

TW Temperature Warning: the chip temperature exceeds 130°C

TSD1 Thermal shutdown #1: The chip temper: The

1	0	VBat-standby, a readout is not possible, as V1 is off
1	1	Flash Mode

R2 R1 R0	Number of unsuccessfully restarts after thermal shutdown
WD3 WD2 WD1 WD0	Number of Watchdog time-outs (1)
TRIG	Status of the Trigger bit from Control Register 0
SHT_GND	LIN Short to ground
SHT_BAT	LIN Short to battery
DOM_TXD	Dominant TXT
RES	Reserved

1. Bits are cleared at every valid WD trigger or when forced sleep mode is entered (after 15 WD failures have been detected)

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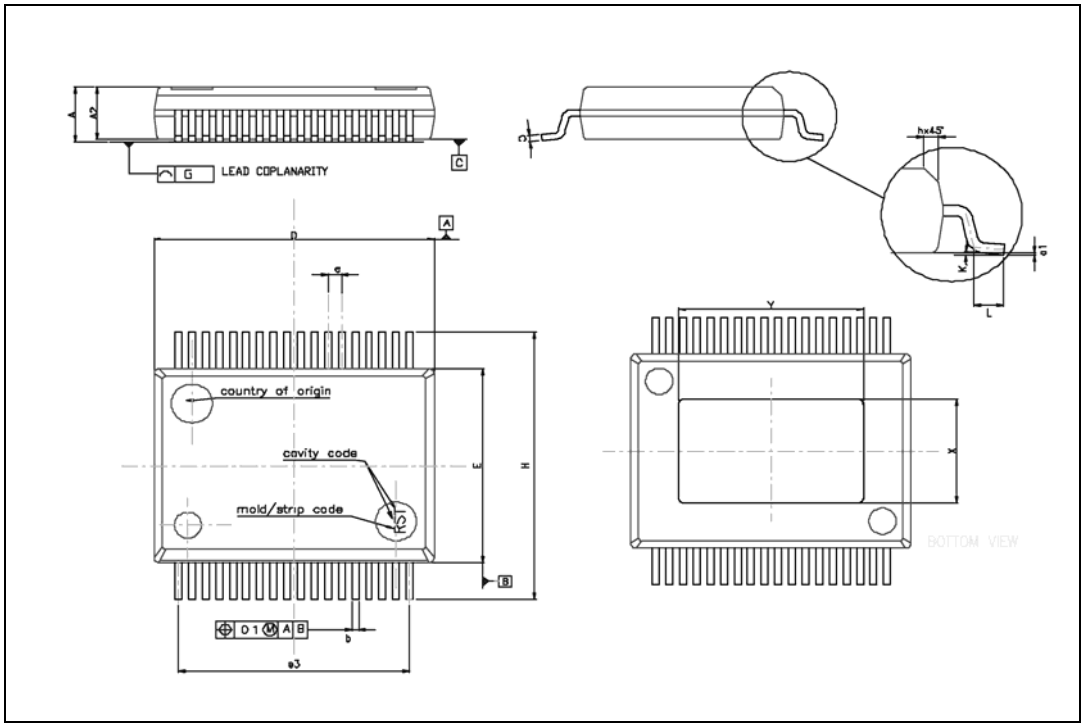
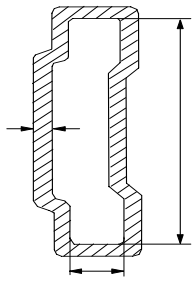


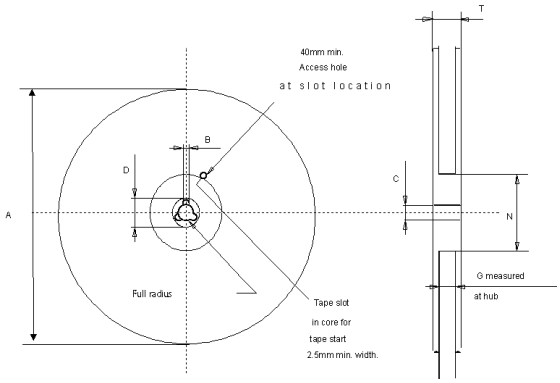
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32

D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10 deg
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1.0	-
X	4.1	-	4.7
Y	6.5	-	7.1



	49
	1225
	532
	3.5
	13.8
	0.6

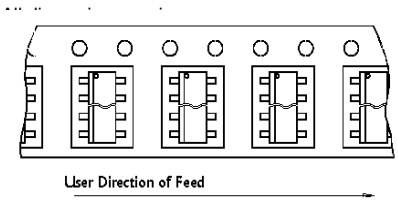
All dimensions are in mm.

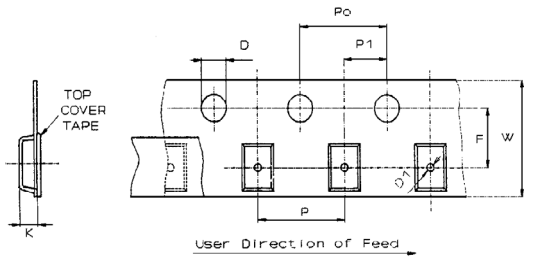


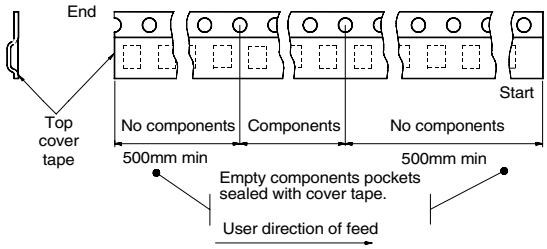
	1000
	1000
	330
	1.5
	13
	20.2
	24.4
	100
	30.4

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

		24
		4
		12
		1.55
		1.5
		11.5
		2.85
		2







24-Aug-2007	1	Initial release.
07-Sep-2007	2	*Table 18: High side outputs (OUT 1..4)*: modified openload detection current 1 parameter value (item 7.8.13). *Table 20: Wake up inputs(WU1...WU4)*: modified Input current in standby mode test condition (item 7.10.5). *Table 22: LIN receiver*: modified symmetry of transmitter propagation delay time parameter value (item 7.12.24). Added *Section 9.3: PowerSSO-36 packing information*.
21-Sep-2007	3	*Section 7.2: Oscillator*: changed Vs minimum value from 7 to 6 V. *Table 10: Supply and supply monitoring*: – changed parameter 7.1.10 ($I_{V(BATWU)}$) max value from 300 to 320 µA – changed parameter 7.1.11 ($I_{V(BATWU)}$) max value from 380 to 410 µA.
11-Apr-2008	4	Modified *Figure 4.: Watchdog* Modified *Section 2.13: Low side driver outputs Rel1, Rel2*. Added note to *Section 2.2.2: Flash mode*. *Section Table 48.: Control register 2*: changed definition to V_S Lock Out parameter. Added *Section 6.3: Package and PCB thermal data*. Modified *Section 7.14.3: Input PWM 2 Vth for flash mode*. *Table 42: Control register 1*: modified "pull down" settings for the wake-up inputs WU1..4 .
08-Jul-2009	5	*Table 60: PowerSSO-36 mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added k row – Changed G (max) value from 0.075 to 0.1

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